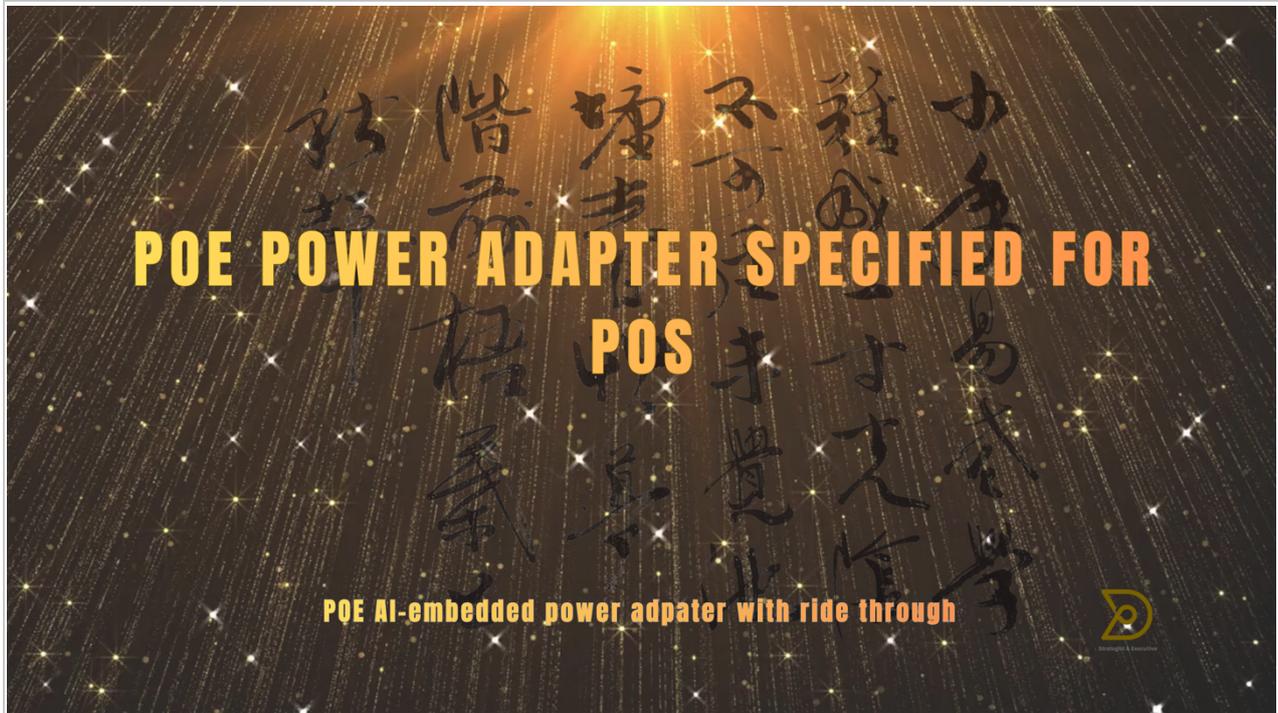


# XR-VPP AI-POWER- ADAPTER SPECIFICATION



**Series:** XR Series / XR Ecosystem Product #2 (after PNL COO)

**Document No.:** XR-VPP-SPEC-001

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**Date:** January, 08, 2026; **Author:** Dennis TY. Leo

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3. Power governance, evidence logging, drift-aware sequencing/derating policies
4. Compliance-bound system delivery and certified pairing strategy
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# 1 EXECUTIVE SUMMARY

**Retail POS is a deployment business before it is a hardware business.**

Across thousands of stores, the biggest operational cost is not the bill of materials—it is the friction of installation, cable management, power stability, and field service.

Today's POS deployments suffer from three chronic problems:

**Power clutter and inconsistent installation quality** — multiple adapters, loose cables, and unmanaged routing under stands or arms create failure points and prolong service time.

**Brownout-driven reboot and transaction disruption** — brief power sags, port resets, or marginal adapters can trigger unexpected restarts, turning a small electrical event into real revenue loss and customer frustration.

**Zero evidence in the field** — when issues happen, teams have no actionable “power evidence” (sag events, thermal stress, peak patterns). Troubleshooting becomes guesswork, driving NTF/RMA cycles and recurring failures.

**XR-VPP (XR VESA Power Plate) is designed to solve these POS-native problems as a deployable platform.**

It integrates VESA mounting, cable routing, and power governance into a rugged anodized aluminum plate that can serve as both a mounting interface and a counterweight component for POS stands.

The system is built on the Hybrid PoE power principle:

PoE supplies the average power envelope, while an energy buffer provides ride-through and peak support.

This architecture enables a clean “one-cable” installation model without sacrificing user experience during transient events—delivering a no-reboot retail experience under real-world power conditions.

To ensure the product is not merely a circuit but a **deliverable, certifiable, warranty-grade platform**, XR-VPP supports an optional **certified AC-DC system kit** for non-PoE sites and compliance-bound deliveries.

This approach raises the barrier from “copyable power circuitry” to “qualified system delivery.”

**In short:** XR-VPP turns POS power from a commodity adapter problem into a scalable deployment standard—cleaner installs, fewer failures, and evidence-driven service.

## 2 PRODUCT OVERVIEW

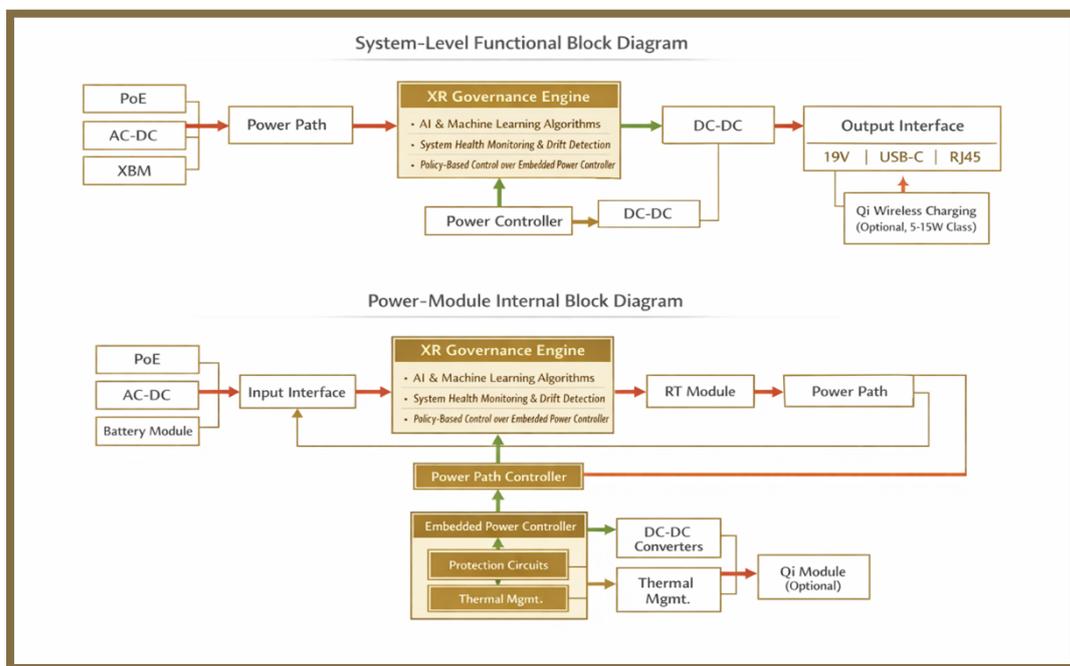
XR-VPP is a **POS-centric power platform** that transforms how power is delivered, buffered, and governed at the edge. It is designed as a plate-form module that integrates cleanly with common POS mechanical ecosystems while providing a modern power architecture that supports **PoE Type-4 worst-case budgets**, optional external DC input, optional external backup, and a ride-through capability that protects transactions and system state during power disturbances.

Unlike conventional adapters that simply output a voltage, XR-VPP introduces an **XR Power concept**: power delivery is treated as a reliability system with **policy, evidence, and learning**. The platform is built to support legacy POS power needs (e.g., 19V rail) while enabling contemporary interfaces such as USB-C, and an optional Qi module when the business case applies.

Two functional block diagrams are provided to communicate feasibility and architecture intent:

A **system-level diagram** showing how XR-VPP fits into POS deployments.

An **internal functional block diagram** describing input arbitration, conversion, ride-through, and governance.



**FIGURE 2-1**

Figures in this document are functional in nature. They are intended to represent feasibility and architectural intent rather than PCB-level wiring or implementation detail.

### 3 KEY FEATURES

- **RT-500 Flagship Ride-Through**  
Provides an extended ride-through window designed to protect transaction continuity and system stability under input dropouts and brownout conditions.
- **Type-4 Worst-Case, Backward Compatible**  
Designed with PoE Type-4 as the worst-case power envelope while maintaining graceful behavior under lower PoE classes and mixed deployment conditions.
- **POS-Native Outputs with Modern Options**  
Supports a 19V legacy rail and introduces USB-C output as an option; Qi is supported as an option module for specific mobile POS workflows.
- **Peak-Aware Power Delivery (Retail Reality Ready)**  
Explicit support for printer-driven transient peak loading behavior without forcing indiscriminate shutdown of other outputs; policy-based throttling is used where required.
- **XR Governance as a Differentiator**  
Adds an orbit-level governance layer that turns power behavior into structured evidence, enabling diagnostics, policy enforcement, and Machine Learning augmentation without compromising deterministic safety.
- XR Confidence Learning for OCP Root-Cause Disambiguation (Inrush vs. Load vs. Sequence)
- XR Confidence Learning for Transient Power Faults — Learns from inrush / sequencing-sensitive OCP events and converts NTF-class trips into repeatable signatures and mitigations.
- Autonomous Boot Convergence (Self-Healing Restart) — Automatically converges to a stable power-up by tuning restart/sequence behavior within safety guardrails; no human intervention required.
- Causality Drift Detection + Evidence Log — Records power events with time-stamped evidence and confidence scoring to enable proactive reliability improvement.
- Safety-First Governance — XR Governance never bypasses hardware protections; it governs recovery and derating policies without compromising safety.

## 4 FUNCTIONAL SPECIFICATIONS

XR-VPP governs power like a reliability system: preserve the POS rail first, shed options next, throttle gracefully, then protect deterministically—with evidence.”

### 4.1 Scope and Functional Intent

XR-VPP is a VESA-mountable external power platform for POS deployments. It consolidates multi-source input power, deterministic power path arbitration, ride-through energy buffering (RT), and XR Governance to deliver **stable primary power** and **managed optional outputs** under real retail transient conditions.

This chapter defines “what the product does” and the functional behavior of each block, independent of reliability targets and regulatory strategy (covered in Chapters 5–7).

### 4.2 Input Sources (Three Options)

XR-VPP supports exactly three input source options. Only one input source is active at a time through power path arbitration.

#### 4.2.1 PoE Input (Worst Case: IEEE 802.3 Type-4; Backward Compatible)

- XR-VPP shall accept PoE input as the **worst-case design point** (Type-4 as the sizing envelope).
- XR-VPP shall be **backward compatible** with lower PoE classes/modes to support mixed deployment environments.
- PoE power is processed internally through the PD function (see 4.4).

#### 4.2.2 External DC Input (via AC-DC Adapter)

- XR-VPP is a DC-DC platform. Therefore, “AC Mains” is treated as **an external AC-DC adapter** providing DC to XR-VPP.
- External DC input may be 12V/19V/24V/48V-class DC (exact ranges defined in Electrical Chapter).
- External DC input is a first-class input option and participates in power arbitration.

### 4.2.3 XBM Input (External Backup Module)

- XR-VPP shall accept an XR-approved external backup module (“XBM”) as a DC input option.
- XBM is a controlled ecosystem accessory; it is not intended as an open battery interface for arbitrary third-party packs.
- XBM connects as a power source option and may also provide its own protection/management on the module side.

## 4.3 Input Interface and Power Path Arbitration (Mux / Path Controller + Power Bus)

### 4.3.1 Power Path Controller (PPC)

XR-VPP shall include a Power Path Controller responsible for:

- Selecting which input option controls the internal power bus
- Providing deterministic arbitration rules (priority and lockout as configured)
- Enabling seamless source switching within defined boundaries
- Enforcing safety limits during source transitions (inrush, surge, brownout handling)

### 4.3.2 Internal Input Power Bus

- After arbitration, the selected source shall feed a single internal **Input Power Bus**.
- The bus is a shared internal rail used by downstream functional blocks (PD path, DC-DC conversion, RT coupling).
- The bus shall never be driven concurrently by multiple sources.

## 4.4 PoE PD Function (Internal)

- The PoE PD function (PD control + isolation as applicable) shall be **inside XR-VPP**, not part of the external source.
- PD function shall interface to the Input Power Bus under control of the Power Path Controller.
- PD behavior (classification/negotiation/limits) shall be consistent with the chosen worst-case envelope (Type-4) while maintaining backward compatibility.

## 4.5 Ride-Through (RT) Buffer and RT-500 Flagship Behavior

### 4.5.1 RT Purpose

RT provides short-duration energy continuity during:

- Micro-drop events / brownouts / source handover
- Transient instability induced by retail loads
- Controlled transition windows when optional outputs are shed or throttled

### 4.5.2 RT-500 Flagship

XR-VPP shall support a flagship ride-through profile:

- **RT-500 @ 65W (steady)** as the primary headline capability.
- RT behavior is verified through Appendix A waveforms.

### 4.5.3 RT Policy Interaction with Outputs

During RT entry/active window:

- The system shall preserve the **primary rail** first
- Optional outputs may be degraded following the policy ladder:
  - Shed Qi (if present)
  - Throttle USB-C to low-power window

User-Perceived Continuity Requirement:

For transient OCP events shorter than the RT window, the system shall recover within the RT-500 continuity envelope such that the host system does not experience a visible power interruption.

Implementation Split:

PEC implements deterministic fast fault recovery (auto-retry with bounded attempts). XR Governance coordinates post-event derating and policy actions to reduce recurrence probability.

## 4.6 DC-DC Conversion and Primary Output

### 4.6.1 Conversion Function

XR-VPP shall convert from the internal Input Power Bus to the primary output domain via high-efficiency DC-DC conversion.

### 4.6.2 Primary Output Requirement

- **19V output** shall be supported as the primary legacy-compatible POS rail.
- Nominal regulation target: **19V ±5%** (final boundary conditions defined in Electrical Chapter).

## 4.7 Optional Outputs (USB-C and Qi)

### 4.7.1 USB-C Option

- USB-C output is optional and may be enabled by SKU/configuration.
- USB-C shall support an **RT window throttle / low-power mode** to protect primary rail continuity during RT or peak events.
- USB-C is treated as a secondary-priority rail under governance policies.

### 4.7.2 Qi Wireless Charging Option

- Qi is optional and implemented as a modular or configurable function.
- Qi shall be the **first output to shed** under RT or peak stress conditions to preserve system stability.
- Qi operation shall be governed by thermal and power budget policies (detailed in Governance chapter and Appendix A).

## 4.8 Peak Load Support (Preset A; Printer-Oriented)

POS deployments frequently drive transient peaks (e.g., printers during dense print patterns). XR-VPP shall support peak behavior defined by **Preset A**:

XR-VPP AI-embedded Power Adapter RFQ

- 72W is treated as the **steady-state rating**.
- XR-VPP shall also support a defined **transient peak ceiling** to avoid unnecessary feature shutdown during short peaks.
- Peak behavior and pass/fail waveforms are defined in Appendix A (Peak Profile, Preset A).

Policy behavior under peak:

- Shed Qi first
- Throttle USB-C next
- Preserve 19V rail continuity and recovery

## 4.9 Embedded Power Controller (EPC) — Deterministic Device

### Operation

XR-VPP shall include an Embedded Power Controller that:

- Executes deterministic sequencing and state control of the power system
- Interfaces to protection and sensing (thermal, bus status, pre-fault indicators)
- Enforces safe operating behavior independent of XR Governance presence

**Design principle:** Removing XR Governance shall not prevent device operation. The EPC ensures baseline functionality.

### 4.10 XR Governance (Functional Interface View)

XR Governance is an intelligence layer operating above EPC. Functionally, it shall:

- Observe key power health indicators and event signatures
- Apply a policy ladder to protect continuity and stability
- Generate structured logs suitable for reliability analytics and ML training

Detailed XR Governance architecture, algorithm + machine learning boundaries, causality drift, and dataset generation requirements are specified in the XR Governance Chapter (next deliverable).

### 4.11 Functional Block Descriptions (One-Line per Block)

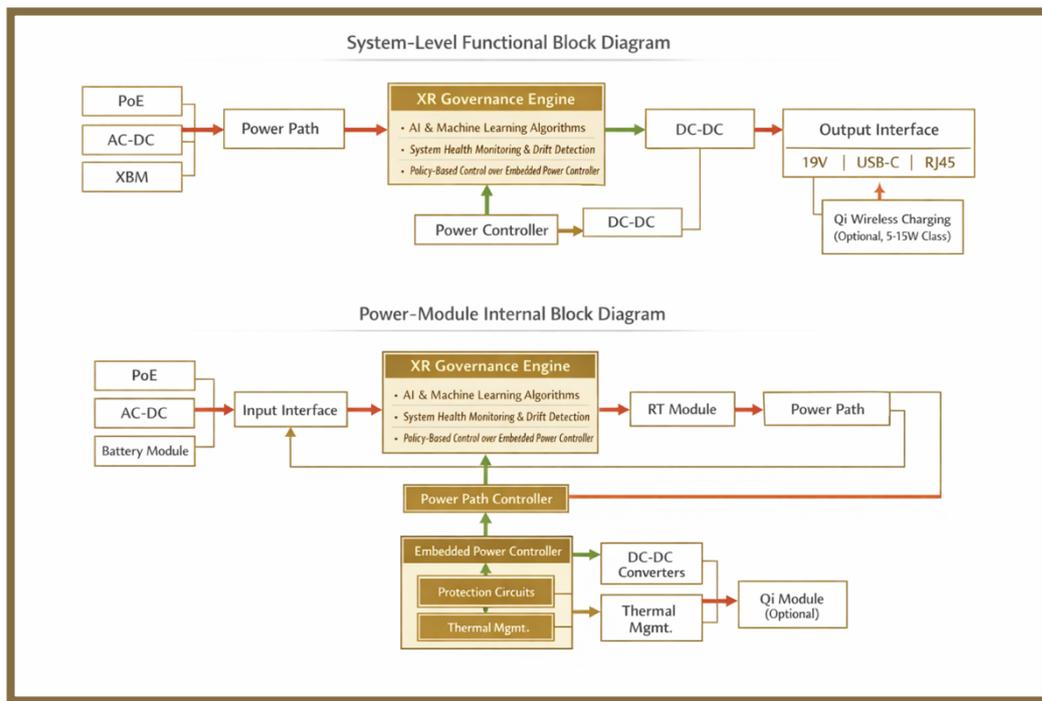


FIGURE 4-1

- **PoE Source:** external PoE switch/injector providing power over Ethernet
- **External DC Source (AC-DC):** external adapter providing DC into XR-VPP
- **XBM:** XR-approved external backup power module (controlled ecosystem input)
- **Power Path Controller (Mux/Arbitration):** selects active source and protects transitions
- **Input Power Bus:** internal shared rail driven by the selected source
- **PoE PD Function:** internal negotiation/control/isolation for PoE power extraction
- **RT Buffer:** internal energy buffer enabling RT-500 continuity behavior
- **DC-DC Conversion:** high-efficiency conversion to primary 19V domain
- **EPC:** deterministic embedded controller for baseline operation and safety sequencing
- **XR Governance:** causality drift detection, policy actions, logging, and ML dataset generation
- **Outputs:** 19V primary output + optional USB-C + optional Qi (policy-managed)

## 4.12 Mechanical Design Specification

### (XR-VPP Plate)



FIGURE 4-2

#### 4.12.1 Mechanical Overview

XR-VPP is implemented as a **fanless plate-form power module** for POS terminal ecosystems, supporting three primary use scenarios:

- VESA-mounted behind POS display (hidden cabling, serviceable access)
- Mounted under POS base as a counterweight plate (sleek, low-profile appearance)
- Desktop placement as a standalone power/charging base (Qi optional)

The mechanical design shall support:

- Clean integration with POS mounting conventions (VESA 75/100 intent; hole pattern defined later)
- Hidden cable routing through the central cavity (no “beard” wiring on outer edges)
- Robust connector retention and strain relief by mechanical structure (not relying on PCB solder joints)
- Safety-driven touch and insertion constraints
- Plate-based thermal spreading without forced airflow

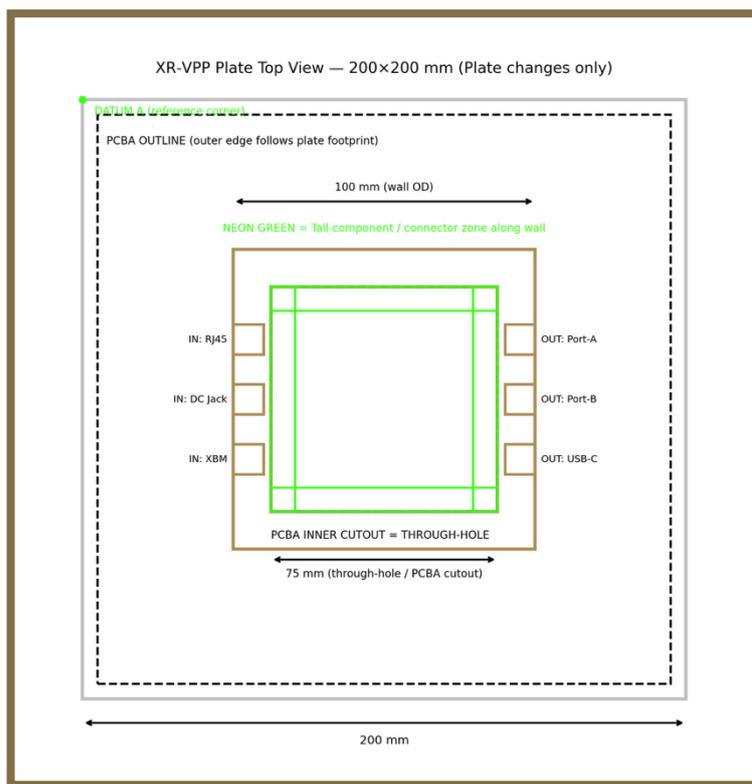
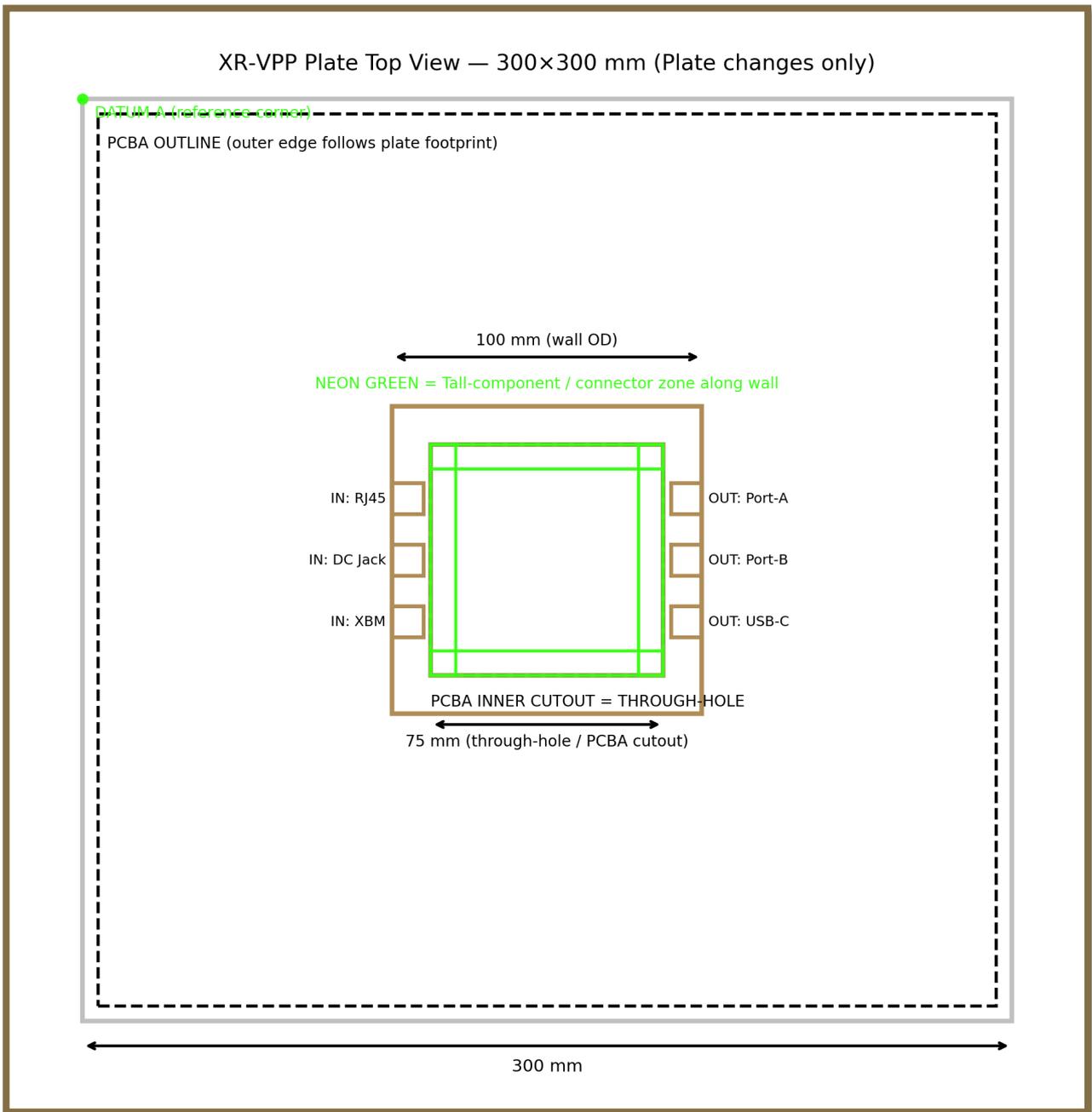


FIGURE 4-3

- Optional Qi module integration without permanently embedding the coil in the plate



**FIGURE 4-4**

## 4.12.2 Envelope and Datum Definition

### 4.12.2.1 Envelope Dimensions (Dream Spec; to be frozen at Industrial Design Release)

XR-VPP shall have two industrial design variants:

#### Variant A — Compact Plate

- Outer dimensions: **200 mm × 200 mm**

## XR-VPP AI-embedded Power Adapter RFQ

- Base plate thickness: TBD (recommended ~8–12 mm class)
- Top cover thickness: TBD
- Central wall height: TBD
- Mass target: TBD

### Variant B — Large Plate

- Outer dimensions: **300 mm × 300 mm**
- Base plate thickness: TBD
- Top cover thickness: TBD
- Central wall height: TBD
- Mass target: TBD
- Notes
- Variant A is intended as the “POS realistic” baseline.
- Variant B provides extra margin for cable bend radius, connector pocket depth, and thermal spreading.

#### 4.12.2.2 Datum and Coordinate System

All I/O locations and mechanical callouts shall reference a consistent datum system:

- Datum origin at **geometric center** of the plate (preferred for symmetry)
- Datum plane Z0: primary mounting surface (the “flat back” face)
- Mechanical drawings shall specify connector centerlines as X/Y coordinates from datum center, and insertion direction relative to Z.

#### 4.12.3 Central Through-Hole + Podium Wall Geometry (Structural Core)

XR-VPP uses a **true through-hole** at the center, with a **podium wall ring** rising from the top cover. This architecture is mandatory to ensure:

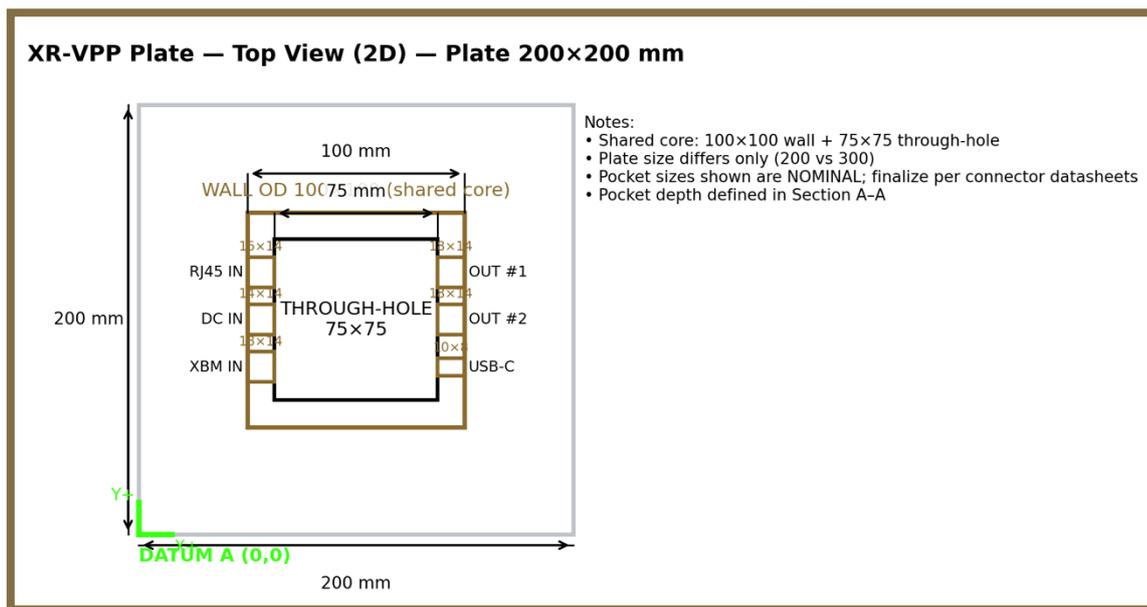
- Hidden cable routing through the center (no external wire exposure)
- Mechanical retention volume for connectors
- Encapsulation of tall power components (“Power board” zone) inside the wall volume
- Support for Qi pad mounting in desktop mode



**FIGURE 4-5**

**4.12.3.1 Variant A (200 × 200) — Through-Hole and Wall**

- Central through-hole opening (inner boundary): 75 × 75 mm (rounded corner fillets, large R)
- Podium wall outer boundary: 100 × 100 mm
- Wall thickness: 25mm per side

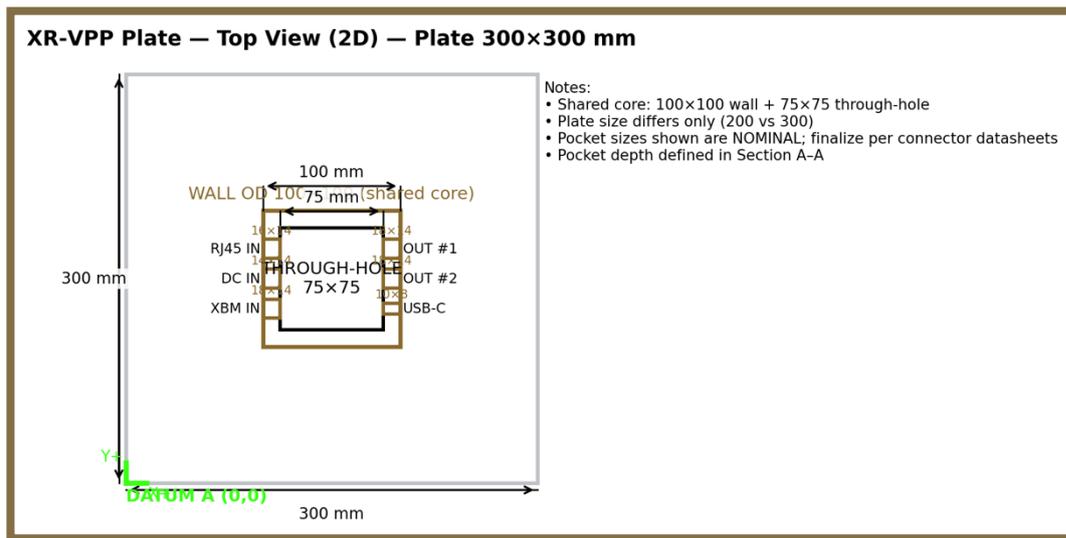


**FIGURE 4-6**

**4.12.3.2 Variant B (300 × 300) — Through-Hole and Wall**

- The plate is expanded to 300 x 300 mm while the wall keeps identical
- The plate shall have **ONLY two vertical layers**:
  - Base plate
  - Top cover with one podium wall ring

No stepped structures, no secondary raised stages, and no additional terraces are allowed.



**FIGURE 4-7**

#### 4.12.4 Construction and Assembly (Base Plate + Top Cover)

XR-VPP mechanical construction shall follow a two-part enclosure concept:

- **Base Plate (BP):** structural aluminum plate, primary thermal spreader
- **Top Cover (TC):** carries the **podium wall ring** and defines the internal cavity walls and connector pockets

Assembly intent:

- BP provides stiffness, heat spreading, and mounting base
- TC provides the wall ring volume to contain tall components and stabilize connectors
- Through-hole passes fully through BP + TC

#### 4.12.5 I/O Placement, Connector Pockets, and Mechanical Protection



- Anti-rotation / anti-wobble stability
- Load transfer from insertion/cable bending into the wall (not into solder joints)
- Repeatable alignment and seating feel

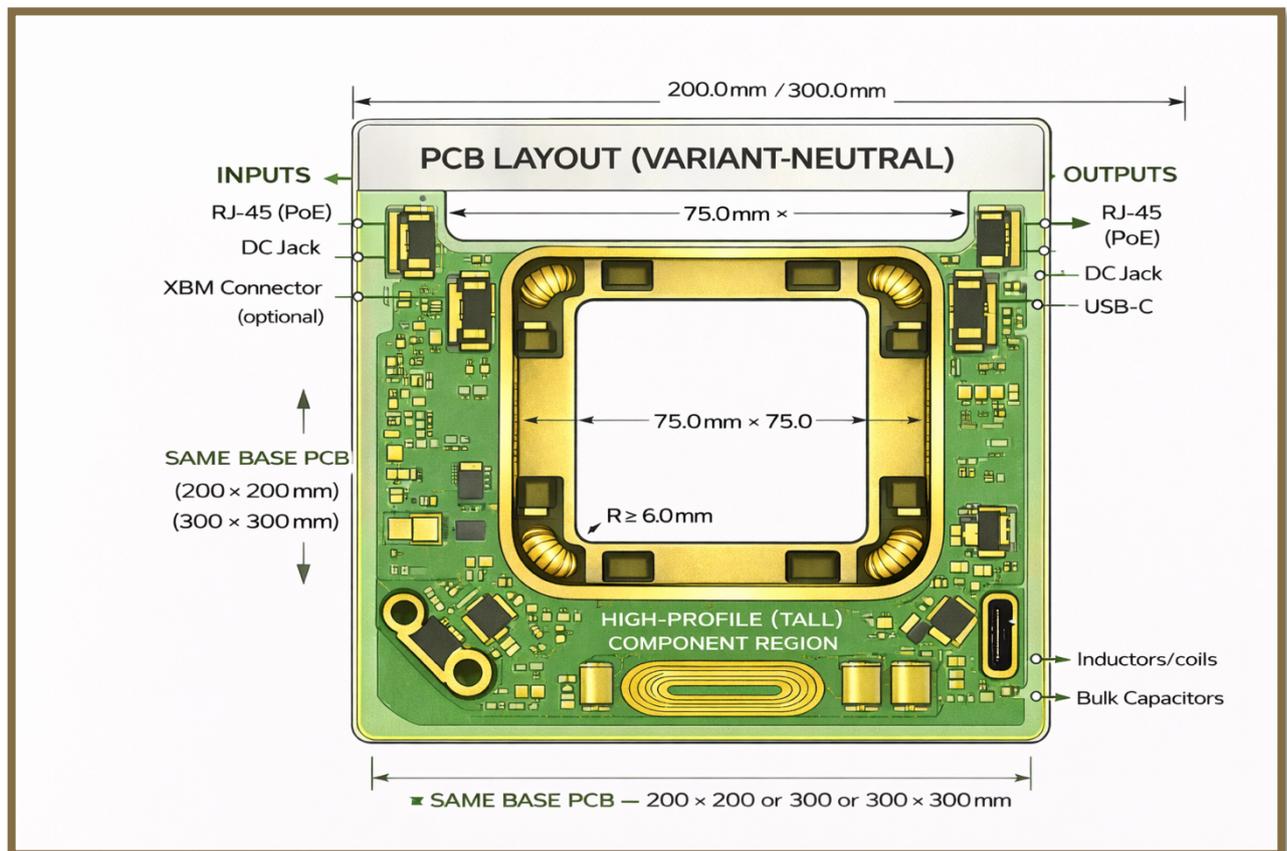
Pocket definition per connector

- $PW_i$ : pocket width
- $PH_i$ : pocket height
- $PD_i$ : pocket depth
- $PR_i$ : corner radius
- $PS_i$ : optional shoulder/step geometry

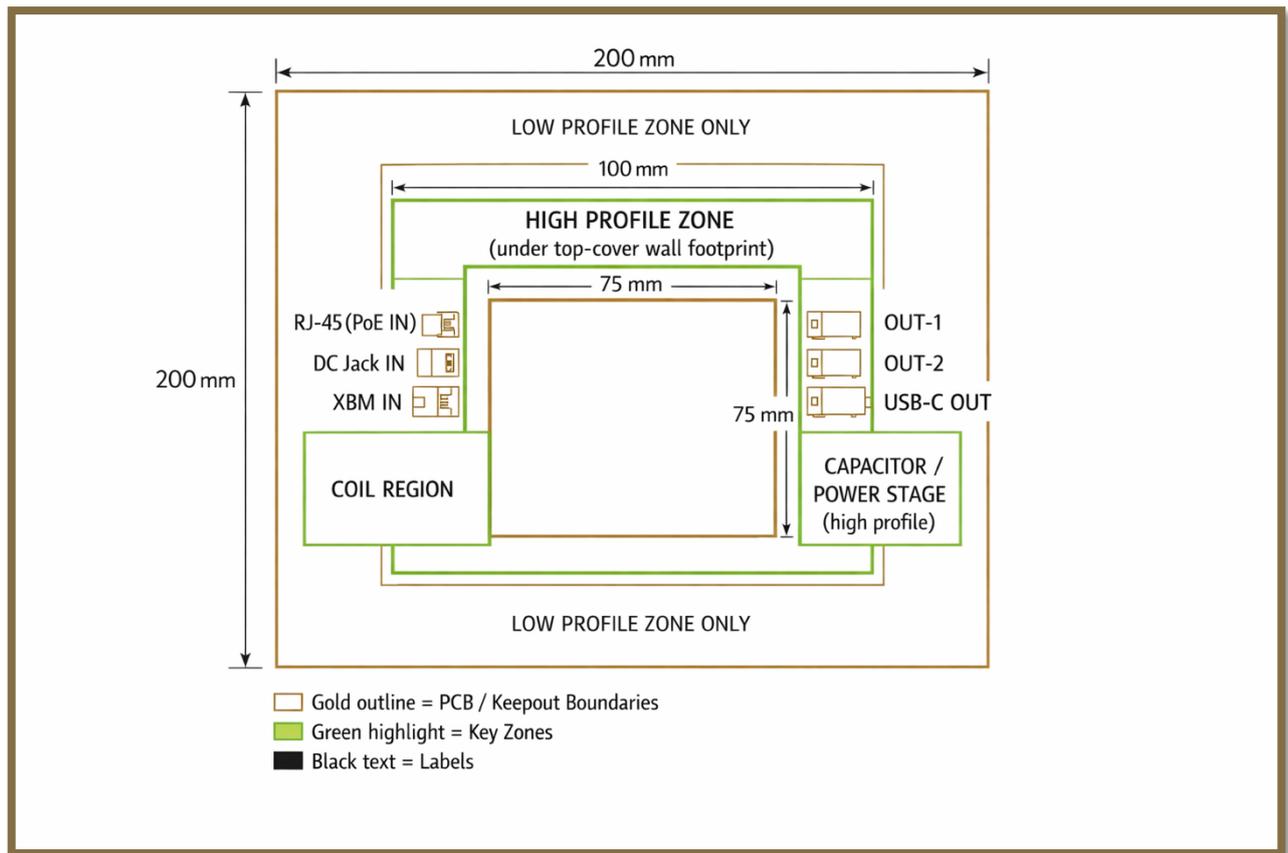
**Top-View Shadow Requirement (“Shared Shadow”)**

From top view, the connector pocket intrusion shall be visible as a **recess shadow feature** on the wall ring, so reviewers can confirm the connector retention concept from 2D drawings.

**4.12.6 4.5.6 PCBA Mechanical Volume and Zoning (PowerBall + IO Corridor)**



**FIGURE 4-9**



**FIGURE 4-10**

XR-VPP internal layout shall be described as two mechanical zones:

**4.12.6.1 Zone P — Power board Volume (Tall Components)**

Located within the podium wall ring volume, containing:

- Inductors / coils
- Bulk capacitors
- tall power components

**4.12.6.2 Zone IO — IO Corridor (Connector + Routing)**

Located adjacent to connector pockets, containing:

- connector solder tails
- IO routing region
- mechanical retention interfaces

**Hard rule:** Tall Power board components shall not overlap the IO corridor in plan/height. IO placement must be mechanically offset from tall components.

A 2D board outline drawing shall be provided in the mechanical appendix, including:

- PCBA X/Y size (TBD)
- Power board zone boundary (shaded region)
- IO corridor boundary
- connector interface mapping

#### **4.12.7 Qi Wireless Charging Option (Detachable Module)**

Qi is an optional accessory and shall not be embedded into the base plate.

- When present, Qi pad sits on top of the podium wall
- Qi pad can be larger than the through-hole opening in X/Y
- Qi wiring routes downward into the through-hole and is visually hidden
- When not used (VESA mount mode), the central through-hole is open for cable routing

#### **4.12.8 Surface Finish, Durability, and Safety**

- Base material: anodized aluminum (grade TBD)
- Finish: brushed anodize appearance; brand color options TBD
- All user-touch edges deburred; chamfer/radius TBD
- Hazardous nodes shall not be finger accessible under normal use
- Marking zones reserved for regulatory labels, serial number, revision ID (per Chapter 7)

#### **4.12.9 Thermal Mechanics (Fanless Plate Dissipation)**

- Base plate is the primary heat spreader
- No fan assumed
- Thermal validation scenarios include: behind display / under base / tabletop
- Hot-zone labeling strategy defined during DV if touch temperature limits require it

## 4.13 Power Embedded Controller Specification (PECS)

### 4.13.1 Baseline Requirement (AI-Independent Operation)

The Power Embedded Controller (PEC) is the mandatory real-time authority for safe and functional operation.

**Normative requirement:** XR-VPP shall remain fully functional (power delivery + protection + RT baseline behavior) when XR Governance is disabled or absent.

### 4.13.2 Responsibilities

The PEC shall:

- Detect available input sources and validate voltage/stability windows
- Coordinate power path arbitration and safe switching sequences (Mux/Path arbitration)
- Control conversion enable sequencing and power-good supervision
- Enforce deterministic protection behaviors (OCP/OVP/UVLO/OTP/surge/inrush)
- Coordinate ride-through entry/exit and baseline buffering behavior
- Generate minimal event logs (“power SMART”) for traceability
- **Own and execute power sequencing (power-up/down) as the authoritative real-time layer**
- Manage I/O enable policies consistent with mechanical constraints (connector retention zones / cable load constraints do not alter safety enforcement)

### 4.13.3 Operating State Machine

Minimum state machine:

- INIT: configuration load, sensor sanity checks
- SOURCE\_DETECT: detect and qualify PoE / External DC / XBM
- ARBITRATE: select one valid input source under priority rules
- PRECHARGE/INRUSH\_CONTROL: stabilize bus, limit inrush
- POWER\_ON: enable conversion stages and outputs in defined order
- RUN: steady-state delivery with monitoring
- PEAK\_EVENT: peak load response coordination (policy hooks)
- RT\_EVENT: ride-through response coordination

- FAULT: protective behavior (hiccup/latch/retry rules)
- SAFE\_SHUTDOWN: controlled disable + event closure

State transitions shall be triggered by measurable conditions with defined debounce/time windows.

#### **4.13.4 Input Arbitration and Power Path Control**

- Only one source shall occupy the primary internal DC bus at a time, unless explicitly defined as controlled assist.
- Arbitration shall consider source validity, thermal headroom, and protection limits.
- PEC coordinates with the Power Path Controller to ensure no unsafe switching under load.

#### **4.13.5 Deterministic Protection Behavior**

Protection handling shall be deterministic and configurable per SKU:

- OCP: threshold + response (limit/hiccup/latch)
- OVP/UVLO: threshold + debounce + recovery
- OTP: derate → protect → shutdown strategy
- Surge/inrush: controlled enable + record fault causes

No oscillatory behavior is allowed under repeated fault conditions.

#### **4.13.6 Power Sequencing Ownership and Adjustability**

PEC is the sole executor of power sequencing (rail enables, soft-start behavior, output bring-up order, power-good gating).

Sequence parameters may be configurable (per SKU and per policy) within PEC guardrails, including:

- soft-start slope selection
- enable delay windows
- restart cadence
- output priority / derating policy hooks (e.g., USB-C throttle, Qi disable)

**Rule:** Known and reproducible timing issues identified during DV shall be resolved as Design Specification updates, not deferred to field tuning.

#### **4.13.7 Minimal Telemetry and Logging (Non-AI)**

The PEC shall record:

- power cycles and runtime counters
- input source change events
- RT entry/exit and duration
- peak event markers (where supported)
- fault type, impacted rail, timestamp

Logs shall be internally persistent; export may be mediated by XR Governance when present.

#### **4.13.8 Interface to XR Governance (Policy, Not Direct Actuation)**

XR Governance shall not directly control power stages. XR Governance issues policy directives to PEC such as:

- output priority policies
- throttling requests (e.g., USB-C low-power throttle)
- optional feature disable (e.g., Qi off)
- safe-state entry requests

PEC enforces safety constraints and may refuse directives that violate protection boundaries.

#### **4.13.9 PEC Firmware Architecture (Code Structure Requirements)**

PEC firmware shall follow a modular architecture:

- Boot & Update (versioning / rollback if applicable)
- HAL & Drivers (ADC, current sense, GPIO, PWM, I<sup>2</sup>C/SPI/UART, NVM, watchdog)
- State Machine Core (INIT → RUN → FAULT)
- Protection Manager (OCP/OVP/UVLO/OTP, debounce, classification)
- Sequencing Manager (rail order, PG gating, restart cadence)
- Ride-Through Manager (entry/exit criteria, timers, buffer status)
- Peak Event Manager (short window peak handling hooks)

## XR-VPP AI-embedded Power Adapter RFQ

- Telemetry & Event Log (“power SMART” format)
- Policy Mailbox Interface (XR Governance directives + accept/refuse reporting)

## 5 XR GOVERNANCE ARCHITECTURE AND INTELLIGENCE LAYER

XR Governance bridges deterministic power safety and field reliability evolution.

The XR-VPP architecture separates responsibilities into two layers: a deterministic Power Embedded Controller (PEC) that executes safety-critical protection and sequencing, and an XR Governance layer that performs evidence-driven learning and policy supervision. This partition ensures that the device remains safe and operable even when XR features are disabled, while enabling continuous reliability improvement when XR is enabled.

### 5.1 Role and Positioning of XR Governance

XR Governance is a **higher-orbit intelligence layer** operating on top of the Embedded Power Controller (EPC).

Its purpose is not to replace deterministic control, but to **observe, learn, predict, and intervene before failure occurs**.

#### Design axiom:

XR Governance is additive, not substitutive.

If XR Governance is removed, XR-VPP shall remain fully functional under EPC control.

This separation ensures:

- regulatory compliance
  - deterministic safety
  - architectural credibility
- while allowing intelligence to evolve independently.

### 5.2 Governance vs. Embedded Control (Clear Boundary)

#### 5.2.1 PEC vs XR Governance — Responsibility Partition

Power Embedded Controller (PEC) is the real-time, safety-critical control layer. It is responsible for protection enforcement, sequencing execution, and bounded fault recovery.

XR Governance is the supervisory intelligence layer. It does not directly bypass hardware protection behavior; instead, it learns from field evidence and selects/tunes allowable operational policies within PEC-enforced guardrails.

## 5.2.2 Non-Negotiable Safety Constraint (Hard Rule)

**PEC protection constraints are non-negotiable.** Hardware safety protections—including **OCP / OVP / UVLO / OTP**, surge handling, and inrush limiting—shall remain authoritative at all times.

**XR Governance shall not override, suppress, bypass, or relax PEC safety limits**, nor shall it modify safety-critical state machines or protection thresholds.

## 5.2.3 What XR Governance *Is Allowed* to Do (Self-Healing Without Overriding Safety)

When transient events occur (for example, inrush-triggered OCP or sequencing-sensitive trips), XR Governance may improve stability by applying recovery and derating strategies **without changing protection thresholds**. Permitted actions include:

Selecting or tuning **restart and sequencing behavior** within the safe parameter space defined by PEC (e.g., restart cadence, sequencing delays, soft-start profile selection).

Applying controlled derating policies to preserve stability and critical operation (e.g., **USB-C throttling, Qi disable**) when peak-load overlap is detected.

Building an evidence-based log (time-stamped events, signatures, outcomes) and maintaining a **confidence score** on mitigation effectiveness.

## 5.2.4 Eliminating the “Design-Time Paradox”

XR self-healing is designed for **unknown deployment variance / NTF-class interactions** that are not fully characterizable at design time (differences in peripherals, cable impedance, connector aging, temperature, supply characteristics, and load transients).

Any timing issue that is clearly reproducible and known during design verification shall be resolved as a **Design Specification** update—through sequence definition, component sizing, and protection coordination—rather than being deferred to field tuning.

**TABLE 5-1**

Layer	Responsibility	Nature
Embedded Power Controller (EPC)	Sequencing, protection, safety limits, hard interlocks	Deterministic / rule-based
XR Governance	Drift detection, policy optimization, predictive intervention	Algorithmic + Machine Learning

XR Governance **never directly drives power devices**.  
 All actions are executed through EPC-approved command interfaces.

### 5.3 XR Governance Functional Objectives

XR Governance is designed to address limitations of traditional power systems:

- **Detect degradation before failure**
- **Distinguish transient stress vs. structural drift**
- **Act early, not after outage**
- **Generate reusable reliability intelligence**

This transforms XR-VPP from a power device into a **reliability instrument**.

### 5.4 Causality Drift Framework

XR Governance continuously observes multi-dimensional feature vectors, including but not limited to:

- RT charge / discharge slope deviation
- capacitor ESR trend shift
- thermal response latency
- peak-load recovery envelope distortion
- PD negotiation retry anomalies
- USB-C throttling frequency under identical workloads

A **causality drift event** is declared when:

A statistically stable functional relationship deviates beyond its learned envelope under equivalent boundary conditions.

This is fundamentally different from threshold-based alarms.

## 5.5 Algorithm + Machine Learning Coexistence Model

XR Governance explicitly consists of **two inseparable halves**:

### 5.5.1 Algorithmic Layer (Deterministic Intelligence)

- Known-safe envelopes
- Physics-based constraints
- Policy ladders
- Rule-guarded actions

This layer guarantees explainability and regulatory defensibility.

### 5.5.2 Machine Learning Layer (Adaptive Intelligence)

- Learns deviation patterns over time
- Refines drift envelopes
- Correlates multi-variable degradation signatures
- Supports cross-unit and cross-deployment learning

**Key principle:**

ML does not decide *what is safe* — it learns *what is changing*.

## 5.6 Policy Ladder (Action Hierarchy)

XR Governance operates using a **Policy Ladder**, ensuring proportional response:

- Log-only (silent learning)
- Soft mitigation (USB-C throttle, Qi shed)
- Load rebalancing
- RT window extension / contraction
- Predictive maintenance flag
- Operator notification / service action

No single anomaly causes immediate disruption unless EPC safety limits are reached.

## 5.7 Reliability Amplification via Governance

Traditional power systems improve reliability by **overdesign**.

XR Governance improves reliability by **early correction**.

Examples:

- Capacitor aging detected before ripple exceeds tolerance
- Thermal resistance drift corrected before derating triggers
- RT profile adjusted before brownout causes reboot

**Result:**

- Extended MTBF
- Reduced unplanned outage
- Controlled degradation instead of abrupt failure

This chapter intentionally bridges into the Reliability Chapter.

## 5.8 Data, Logs, and Ownership (Critical)

XR Governance generates structured datasets including:

- Drift vectors
- Policy decisions
- Pre-failure signatures
- Intervention outcomes

These datasets are:

- **Independent of hardware ownership**
- **Portable across platforms**
- **Reusable across future XR products**

Architectural fact:

- The value of XR Governance increases with deployment scale, not unit margin.
- This makes XR Governance a fundable asset, not a BOM item.

## 5.9 XR Governance as a Testable Engineering System

XR Governance behavior is validated through:

- Controlled RT waveform deviation
- Peak-load stress injection
- Policy ladder response verification
- Cross-run reproducibility

Test vectors and acceptance criteria are defined in **Appendix A**.

This ensures XR Governance is:

- Auditable
- Certifiable as a system
- Defensible in supplier qualification

## 5.10 Strategic Implication (Non-Marketing Statement)

XR Governance enables:

- Power systems that **age gracefully**
- Redundancy without brute-force oversizing
- AI adoption without surrendering safety control

It represents a **new class of power infrastructure intelligence**, not an accessory feature.

## 6 FIRMWARE SPECIFICATION

### 6.1 Purpose and Scope

This chapter defines the **firmware architecture, ownership boundaries, deliverables, and implementation requirements** for XR-VPP. It covers four firmware domains:

- **PEC Firmware (Power Embedded Controller)** — mandatory real-time control plane; AI-independent operation.
- **USB-C PD Firmware** — USB-C power delivery negotiation and power role/policy control (as applicable).
- **XR Governance Firmware + Algorithms** — policy orchestration, causality/drift detection, confidence scoring, and supervisory control.
- **Learning / ML Enablement** — data capture, labeling hooks, training pipeline interfaces, model packaging, and safe deployment.

Normative rule: **XR-VPP must operate safely and deliver baseline power functions even when XR Governance and Learning are absent/disabled.**

### 6.2 Firmware Partitioning and Ownership (Who controls what)

#### 6.2.1 PEC is the real-time authority

PEC is the **only** firmware allowed to directly actuate:

- Power path selection / arbitration (source mux)
- Pre-charge / inrush control
- Rail enable/disable sequencing
- Ride-through entry/exit gating
- Protection enforcement (OCP/OVP/UVLO/OTP/Surge/Inrush)

XR Governance **cannot** directly actuate power stages. It may only issue **policy directives**.

#### 6.2.2 USB-C PD FW is a domain controller

XR-VPP AI-embedded Power Adapter RFQ

USB-C PD FW owns:

- PD contract negotiation, PDO/RDO handling
- Role/config policy within the allowed hardware
- Fault handling and negotiated fallback behaviors (in coordination with PEC protection)

USB-C PD FW must expose:

- Negotiated power state and limits to PEC
- Throttling/derating hooks from PEC (and optionally from Governance through PEC)

### 6.2.3 XR Governance is a supervisory layer

Governance owns:

- Causality/drift reasoning logic (rule + model hybrid allowed)
- Confidence learning hooks and evidence selection
- Policy decisions (priority, throttle requests, safe-state requests)
- Telemetry interpretation and action plan generation

Governance must be **non-blocking** to PEC.

### 6.2.4 Learning is a pipeline, not a safety controller

Learning owns:

- Dataset construction from field telemetry and DV logs
- Offline training and evaluation
- Model packaging/versioning/signing
- Controlled deployment into Governance runtime

Learning cannot override PEC protection.

## 6.3 Supplier Deliverables (What the FW team must hand back)

Supplier shall deliver **at minimum** the following artifacts:

**Source code packages**

## XR-VPP AI-embedded Power Adapter RFQ

- PEC firmware source + build project
- USB-C PD firmware source (or integration project, if PD is an IC stack)
- XR Governance runtime source (if supplier implements it) OR integration hooks if customer implements
- Scripts/config for build and version stamping

### Architecture & design docs

- Module diagram of each FW domain
- Interface spec (signals + mailbox messages + timing)
- State machine spec (PEC) including transition table

### Timing & ISR documents

- Interrupt map: priorities, max ISR budget, nesting rules
- Timing profile table: soft-start slopes, enable delays, retry cadence, RT window control

### Test & validation assets

- Unit test list (by module)
- Integration test checklist
- Fault injection plan and expected outcomes
- Golden log examples for key scenarios (RT, peak transient, OCP, brownout recovery)

### Versioning

- Semantic versioning scheme (FW\_VER)
- Profile ID and configuration checksum included in logs
- Reproducible build instructions

## 6.4 PEC Firmware Specification (Implementation-Executable)

### 6.4.1 PEC Functional Responsibilities

PEC shall implement:

- Source detect/qualify (PoE / DC jack / XBM)
- Deterministic source arbitration and switching
- Inrush limiting and pre-charge

## XR-VPP AI-embedded Power Adapter RFQ

- Rail sequencing (19V + USB-C + optional Qi)
- Ride-through baseline control (RT-500 window as flagship)
- Peak transient mode handling (e.g., printer black-page events)
- Protection handling: OCP/OVP/UVLO/OTP/surge/inrush
- Event logging (“power SMART” minimal persistent log)

### 6.4.2 PEC Operating States (State Machine)

PEC shall implement a **finite state machine** with measurable transition criteria:

- INIT
- SOURCE\_DETECT
- ARBITRATE
- PRECHARGE\_INRUSH
- POWER\_ON
- RUN
- PEAK\_TRANSIENT
- RT\_WINDOW
- FAULT
- SAFE\_SHUTDOWN

Supplier must provide:

- State diagram
- Transition table: trigger condition, debounce window, action, timeout, failure path

### 6.4.3 Real-Time Requirements

- Protection response is deterministic and bounded
- No blocking calls inside protection ISRs
- Logging in ISR is flag-only; full record write deferred to background task
- Watchdog strategy must be documented (kick policy, recovery)

## 6.5 USB-C PD Firmware Specification (At least 65W)

USB-C PD FW shall support:

## XR-VPP AI-embedded Power Adapter RFQ

- Negotiation up to  $\geq 65W$  output (subject to thermal/protection limits)
- Throttle/derate control commanded by PEC (USB-C low-power mode)
- Safe fallback when rail headroom is insufficient (e.g., RT window active)

### Deliverables:

- PD policy configuration (PDO table)
- Event mapping (contract changes, errors, over-current indications)
- Integration interface to PEC:
  - PD\_CONTRACT\_POWER
  - PD\_THROTTLE\_SETPOINT
  - PD\_FAULT\_STATUS

### Rule:

- PEC may force USB-C to reduce power during RT window or peak transient mode to preserve system stability.

## 6.6 XR Governance Firmware + Algorithm Specification

### 6.6.1 Governance Role

Governance consumes telemetry and logs, and outputs **policy directives** (never direct rail control).

Governance shall implement:

- Drift detection (voltage/current/thermal signature deviation)
- Causality correlation (events  $\rightarrow$  suspected contributors)
- Confidence scoring (how sure the system is)
- Policy decision engine (priority/throttle/optional feature disable)
- Recovery orchestration requests (safe-state entry, retry cadence suggestion)

### 6.6.2 Policy Mailbox Interface (Governance $\rightarrow$ PEC)

Mandatory commands:

- SET\_OUTPUT\_PRIORITY(19V, USBC, QI)

## XR-VPP AI-embedded Power Adapter RFQ

- REQUEST\_USBC\_THROTTLE(level, duration\_ms)
- REQUEST\_DISABLE\_QI()
- REQUEST\_SAFE\_STATE(reason\_code)
- SUGGEST\_RETRY\_PROFILE(profile\_id)

PEC responses:

- ACK / NACK
- NACK\_REASON (violates protection constraints / invalid state / thermal limit)

## 6.7 Learning / ML Enablement Specification (Supplier-Executable)

This section defines what “Learning ready” means without requiring the supplier to build full ML.

Minimum requirements:

- Telemetry schema is stable and versioned
- Event logs include configuration signature + timing profile ID
- Data capture supports:
  - RT events (duration, droop curve)
  - Peak transient events ( $\Delta I/\Delta t$ , droop recovery)
  - Fault classification (OCP/OVP/UVLO/OTP/surge/inrush)
  - Source switching episodes (pre/post waveforms)

Optional (Phase-2):

- Feature extraction hooks
- Model packaging interface (signed model blob + version)
- Runtime confidence output consumed by Governance

Safety rule:

- ML outputs may influence **policy suggestions** only; PEC protection remains absolute.

## 6.8 Firmware Code Architecture Requirements (So they know “how to write it”)

Each FW domain shall use a modular architecture with clear boundaries:

### PEC FW modules

- Boot / Update / Versioning
- HAL & Drivers
- State Machine Core
- Protection Manager
- Sequencing Manager
- Ride-Through Manager
- Peak Transient Manager
- Telemetry & Event Log
- Policy Mailbox Interface

### USB-C PD modules

- PD Stack / Policy Engine
- Contract Manager
- Fault Handler
- PEC Interface Adapter

### Governance modules

- Telemetry Ingest
- Event Correlator
- Drift Detector
- Policy Engine
- Confidence Scoring
- Command Mailbox

Supplier must provide:

- Folder structure
- Module ownership
- Public headers/interfaces
- Build targets

## 6.9 Timing Profile & Tunability (How to handle “multiple timing sets” correctly)

Key principle: **(CHECK FIGURE 9-2 & FIGURE 9-3)**

- **Known timing issues found in DV must be fixed in default spec**, not deferred to “field tuning”.
- Tunability is allowed for resilience, not for compensating known design flaws.

Supplier shall implement:

- PROFILE\_A/B/C (defaults) stored in NVM
- Bounded ranges for each tunable parameter
- Profile switching rules (when allowed, which state required)

## 6.10 Phased Implementation Plan (So supplier can commit)

- **Phase-1 (Mandatory):** PEC FW + USB-C PD FW + logging + RT-500 + peak transient mode (no Governance needed)
- **Phase-2 (Recommended):** Governance runtime (policy mailbox + drift/correlation v1)
- **Phase-3 (Optional):** Learning pipeline integration (dataset hooks + model packaging + update mechanism)

## 7 RELIABILITY ENGINEERING SPECIFICATION (XR-VPP)

### 7.1 Reliability Design Intent

XR-VPP is defined as a **Reliability-Governed Power Platform** for POS deployments, not as a commodity power adapter. The product is designed to ensure **predictable continuity, controlled degradation, and evidence-based recoverability** under real retail operating disturbances (input instability, load transients, thermal accumulation, and peripheral-driven peaks).

Reliability is treated as a **first-class design input** (Design Intent), with two enforcement layers:

- **Embedded Power Controller (EPC)** — deterministic, protection-anchored power sequencing and arbitration.
- **XR Governance** — policy-driven reliability management, logging, and learning loop (algorithm + machine learning).

The reliability objective is not “never fail,” but:

- Fail only within **controlled, deterministic boundaries**
- Generate **structured evidence** for root-cause and continuous improvement
- Preserve the **primary POS rail** as the top service priority

### 7.2 Reliability Operating Envelope

XR-VPP shall operate within a defined, multi-dimensional reliability envelope. The envelope is expressed in behaviors and bounded ranges rather than certification test scripts.

#### 7.2.1 Continuity Envelope

XR-VPP shall maintain POS continuity under:

- Short-duration input disturbances (dropout / sag / switchover)
- Load transients typical of POS peripherals
- Controlled load shedding for optional features

## 7.2.2 Transient Envelope (Peak Handling)

XR-VPP shall tolerate transient peaks beyond steady-state rating within a defined peak window. When peak demands approach system limits, XR-VPP shall apply **policy ladder actions** (option shedding / throttling) before invoking protection shutdown, unless safety boundaries are reached.

## 7.2.3 Ride-Through Envelope (RT Window)

XR-VPP shall provide a governed ride-through window (flagship **RT-500**) to bridge:

- Power dropouts
- Brownouts / sags
- Brief upstream interruptions

During RT, the platform shall preserve the primary rail and apply deterministic degradation on optional outputs when necessary.

## 7.2.4 XR Governance Policy Priority Ladder

This ladder defines the default, governed behavior under constrained conditions (RT window, limited input budget, thermal headroom reduction, or protection pre-trigger).

Priority 0 — Safety Boundaries (Always Enforced by PEC)

- PEC protection constraints (OCP/OVP/UVLO/OTP/surge/inrush) are non-negotiable.
- XR Governance directives shall not override PEC safety limits. XR Governance may request

operational derating or controlled recovery profiles, but shall not suppress or bypass PEC protection triggers.

Priority 1 — Preserve Core POS Operation

- Maintain 19V rail stability as the highest service priority (legacy POS continuity).
- Avoid uncontrolled resets or brownouts on the primary POS rail.

Priority 2 — Shed Optional Loads First (Fast)

- If Qi option is enabled, it shall be the first load to disable under constrained conditions.
- Rationale: optional accessory power shall not compromise POS continuity.

### Priority 3 — Throttle Secondary Outputs (Graceful Degradation)

- If USB-C option is enabled, apply USB-C low-power throttle under defined constraint triggers.
- Throttle shall be policy-driven (not fault-driven) and shall be logged as evidence.

### Priority 4 — Ride-Through Preservation Mode

#### During RT windows:

- Enforce a dedicated RT preservation mode prioritizing:
  - 19V stability
  - Optional load shedding (Qi off)
  - USB-C throttle
- Exit RT mode deterministically based on input recovery thresholds + time debounce.

### Priority 5 — Peak Handling Coordination (Preset A)

Under peak demand events (e.g., printer-related transients):

- Maintain delivery within defined peak envelope limits.
- Allow short-duration droop within acceptance envelopes (Appendix A) provided recovery is within limits.
- If peak persists beyond configured window, apply ladder actions (Qi off → USB-C throttle) rather than immediate shutdown.

### Priority 6 — Controlled Safe-State (Last Resort)

If constraints cannot be satisfied without violating safety boundaries:

- Enter a controlled safe-state via PEC with deterministic shutdown sequencing.
- Record full evidence set: cause codes, rail status, source status, and applied policy actions.

## 7.2.5 Thermal Envelope (Fanless Plate)

XR-VPP assumes a fanless thermal regime consistent with plate-style mechanical design. Reliability behavior shall remain stable under thermal accumulation by:

- Thermal-aware throttling policies (optional outputs first)
- Protection-anchored safe-state if thermal boundaries are exceeded
- Logging and evidence capture for field correlation

## 7.3 Reliability-Oriented Design Features

### 7.3.1 Deterministic Power Arbitration

Multiple power inputs and backup sources shall be arbitrated by EPC-controlled power path management. Only one source shall own the internal bus at a time, with defined switchover logic and evidence logging.

### 7.3.2 Controlled Degradation (Policy-Driven)

XR-VPP shall prioritize continuity over brute shutdown by applying controlled degradation:

- Preserve primary POS rail first
- Shed optional features next (Qi option first)
- Throttle USB-C to low-power window if necessary
- Enter safe-state only as last resort or when safety boundaries require it

This behavior is defined by a policy ladder and executed through EPC + XR Governance.

### 7.3.3 Evidence-Generating Power (“Power SMART”)

XR-VPP shall behave as an evidence-producing platform:

- Every reliability-relevant event (RT entry/exit, peak event, throttle, shed, protection trigger) shall generate a structured record.
- Evidence shall be retrievable via defined interfaces and suitable for fleet analytics.

### 7.3.4 Governance-Enabled Reliability Loop

XR Governance is responsible for:

- Correlating observed signals (rail behavior, thermal, protection near-triggers, source quality) into reliability events
- Selecting and enforcing policy actions through EPC
- Producing a learning dataset enabling future improvements

## 7.4 Failure Mode Awareness and Reliability Responses

XR-VPP explicitly recognizes common field failure modes and defines a controlled response strategy for each category.

### 7.4.1 Input Instability

Examples: dropout, brownout, sag, or unstable upstream supply.

**Response intent:** enter RT window when appropriate, preserve primary rail, log event, recover deterministically.

### 7.4.2 Peak Peripheral Loading

Examples: printer actuation, cutter, heavy black print, IO bursts.

**Response intent:** tolerate within peak envelope; if needed, shed Qi and throttle USB-C before any forced shutdown; log peak event shape and actions taken.

### 7.4.3 Thermal Accumulation

Examples: elevated ambient, constrained mounting, sustained load near rating.

**Response intent:** policy-based derating; maintain predictable behavior; log thermal headroom and actions; safe-state if boundaries exceeded.

### 7.4.4 Protection Pre-Triggers

Examples: near-OCP, near-OTP, surge/inrush edge conditions.

**Response intent:** pre-emptive policy action where possible; never override safety; always log.

## 7.5 Reliability Metrics and Acceptance Philosophy

Reliability acceptance is evaluated through:

- **Behavioral determinism** (repeatable reaction to the same stimulus)
- **Continuity under bounded disturbances** (RT window performance)

- **Peak tolerance with recovery** (Preset A peak profiles)
- **Evidence completeness** (logs with cause → action → result chain)
- **Graceful degradation** (option shedding/throttle before shutdown)

Numeric limits (e.g., droop minima, recovery times, peak window bounds) are defined in the Electrical Specification and validated in the DV Plan.

## 7.6 Reliability Evidence and Data Ownership Boundaries

XR-VPP produces reliability evidence as a core product outcome. Evidence includes but is not limited to:

- Event markers (RT/peak/throttle/shed/protection)
- Timestamped rail summaries
- Source status and arbitration state
- Thermal headroom indicators
- Policy actions applied

### Data ownership boundary (design intent):

- The **XR Governance dataset** and derived models constitute the XR domain and are treated as protected assets.
- The embedded controller firmware supports deterministic operation; XR Governance adds observability and learning capability without being required for basic device operation.

## 7.7 Separation of Concerns (EPC vs XR Governance)

XR-VPP is designed to remain functional with XR Governance removed.

- **EPC (Embedded Power Controller):**  
Mandatory for safe operation. Handles arbitration, sequencing, protection-aligned control, and deterministic behaviors.
- **XR Governance:**  
Higher-orbit layer. Applies reliability policies, generates evidence, and enables algorithm + machine learning improvements.

This separation ensures manufacturability, certification feasibility, and platform longevity while keeping XR Governance as the differentiating core.

## 8 COMPLIANCE & REGULATORY FRAMEWORK (SELLABLE-BY-DESIGN)

### 8.1 Compliance Strategy Overview

XR-VPP is designed for international commercial deployment. Compliance is addressed as a **design constraint** rather than a post-fix activity. This chapter defines the compliance intent and certification path without locking test-lab paperwork details prematurely.

### 8.2 Safety (Product Safety Certification Intent)

The product shall be designed to support certification under applicable safety standards for external power modules and DC power delivery products. Design shall include:

- Reinforced insulation strategy where required
- Creepage/clearance design rules aligned to target standards
- Protective earth strategy if applicable (mechanical plate considerations)
- Abnormal operation and single-fault safety behavior

### 8.3 EMC/EMI (Emissions & Immunity Intent)

XR-VPP shall be designed to meet:

- Radiated/conducted emissions limits appropriate to target markets
- Immunity expectations for retail environments (ESD, EFT, surge as applicable)

Design shall incorporate:

- Input filtering, shielding strategy (plate as EMI aid)
- Grounding/bonding architecture
- Cable/interface EMC considerations

## 8.4 Environmental & Materials Compliance

XR-VPP shall support:

- RoHS compliance
- REACH declarations (as applicable)
- Material declarations for major customers

## 8.5 Labeling, Traceability, and Documentation

The product shall include:

- Model/variant labeling for outputs (19V / USB-C option / Qi option)
- Safety marks placeholder strategy
- Traceable serial/lot identification suitable for field reliability analytics

## 8.6 Compliance-by-Configuration

Because XR-VPP includes options (USB-C, Qi, XBM), compliance shall be defined for:

- Base configuration (19V only)
- Optional configurations (USB-C enabled, Qi enabled)
- Worst-case configuration (all enabled)

## 9 VALIDATION FRAMEWORK

DV Plan Structure, Semantic Alignment & Roadmap Traceability

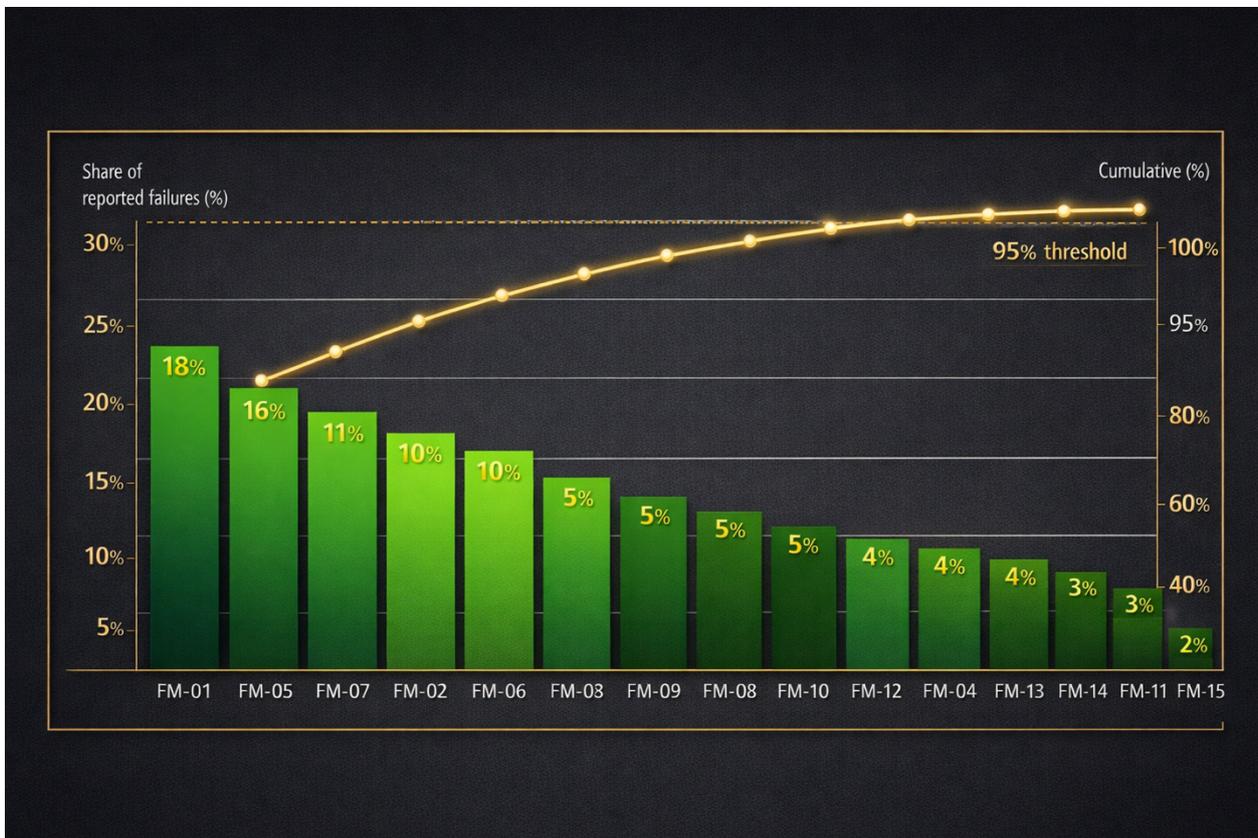


FIGURE 9-1

### 9.1 Purpose and Positioning

#### DV as Design Feedback Engine:

This chapter defines Design Validation (DV) as an engineering control mechanism that produces:

- (1) Qualification-ready, third-party comparable evidence;
- (2) Actionable design feedback to power, firmware, and system architecture teams; and
- (3) AI-ready labeled datasets that enable timing/policy optimization across XR-VPP operating scenarios.

DV in XR-VPP is **not limited to “Power On” and “Power Off.”** Power-on/off are two convenient reference windows to illustrate sensitivity and controllability. The DV framework shall define and validate multiple **scenario-based timing windows** (including transient collision moments) as **first-class controllable objects**, and shall capture evidence in a consistent, comparable format.

DV outputs in this chapter are designed to be **backward compatible** with mature industry semantics used in: transfer switching, redundant power systems, platform management, and power telemetry, to avoid semantic mismatch between supplier test reports, neutral-lab reports, and customer acceptance criteria. This is a **comparability strategy**, not a requirement to rename XR-VPP terms into legacy terms.

**Normative/Informative anchors referenced by DV (non-exhaustive):**

- Transfer switching safety & semantics: UL 1008 (transfer switch equipment scope) ; IEC 60947-6-1 (transfer switching equipment, continuity of supply)
- Power telemetry & device management: PMBus / SMBus (SMIF stewardship)
- Platform management semantics: Redfish (DMTF schemas, including PowerSupply & Redundancy)
- Data center manageability: DCMI specification (built on IPMI)
- Redundant PSU ecosystem reference: OCP M-CRPS base specification

### 9.1.1 Standard/Framework — Purpose in XR-VPP Spec — Application

UL 1008 — Transfer switch equipment safety scope — Source arbitration comparability anchors; evidence collection comparability

IEC 60947-6-1 — Transfer switching equipment (TSE) semantics — Source qualification, stability timing, continuity logic

PMBus / SMBus (SMIF) — Power telemetry & control bus — Device telemetry, configuration, traceability; DV command/electrical integrity

Redfish (DMTF) — Platform schema language — Evidence/event payload projection compatibility (PowerSupply/Redundancy semantics)

DCMI (Intel) — Data center power manageability — Legacy telemetry compatibility projection; power monitoring/control expectations

IPMI (industry spec set) — Base management/event model — Event-log style projection where customer tooling requires it

OCP M-CRPS — Redundant PSU ecosystem reference — DV roadmap alignment; supplier capability migration target

## 9.2 Normative / Informative Anchors

XR-VPP DV is “backward compatible” to mature industrial semantics so the evidence can be audited and compared externally. PMBus / SMBus.

XR-VPP adopts PMBus/SMBus semantics as an **industry anchor for power telemetry and fault vocabulary**, especially for redundancy-grade behaviors and power subsystem observability. PMBus and SMBus are published by **System Management Interface Forum (SMIF)**.

- Use PMBus concepts for: telemetry fields, fault classes, warnings vs faults, status reporting, and command/response expectations.
- Use SMBus as the transport/timing reference for low-speed management bus behavior.

**Supplier requirement:** Even if the XR-VPP does not expose PMBus externally in the baseline product, DV must produce an internal telemetry set that can be **mapped 1:1** into PMBus-style status + sensor concepts for comparability.

### 9.2.1 Platform Management Semantics

Customer-ingestible redundancy language.

Redfish provides structured schema definitions including **PowerSupply** and the common **Redundancy** object used across management resources . DV evidence and event payload projections shall support a Redfish-compatible semantic view so that customer systems can ingest and reason about power health, redundancy, and supply status with minimal re-translation.

For legacy compatibility and auditability, DV shall also support a legacy projection compatible with platform management interfaces used in server ecosystems, including DCMI power-management concepts and IPMI-style event logging where required by customer tooling .

### 9.2.2 Datacenter Redundant Power Supply References

For roadmap alignment and supplier capability migration.

OCP's M-CRPS Base Specification provides a public reference vocabulary for redundant PSU form factors, interfaces, and related expectations . XR-VPP DV shall treat OCP M-CRPS as an **informative reference anchor** so the supplier's DV methods can migrate upward into redundant PSU ecosystems, even if XR-VPP target domain is POS.

### 9.2.3 Transfer Switching Semantics

ATS (Automatic Transfer Switch) systems provide mature and widely-audited semantics for source monitoring, transfer decision logic, transfer sequences, and acceptance testing. XR-VPP does not “rename

itself as ATS,” but leverages ATS logic as a **ground truth reference** for: detection thresholds, transfer triggers, stability windows, and decision logs.

Anchors include:

**UL 1008** scope covering automatic transfer switches and related transfer switch equipment.

**IEC 60947-6-1** Transfer Switching Equipment definition and transfer sequence focus.

**Supplier requirement:** DV must be able to produce logs/evidence that are explainable in ATS-style decision narratives (what was monitored, which threshold was crossed, what stabilization window was applied, what transfer action occurred, and what evidence proves it).

## 9.3 Semantic Alignment and Mapping Table

Canonical Vocabulary for R&D, Lab, Customer, and AI.

### 9.3.1 Canonical term rule

A single observed phenomenon shall map to **exactly one** canonical XR term within this specification. Variants (supplier naming, bench instrument naming, compliance-lab naming, and customer naming) must be represented only as **aliases** mapped to the canonical term. No test report shall introduce new uncontrolled synonyms.

### 9.3.2 Required Mapping Table

Maintained as a living artifact; delivered every DV cycle.

Supplier shall maintain and deliver a **Semantic Mapping Table** that includes at minimum the following columns:

- A. Canonical XR Term (this spec)
- B. Category (Input / Output / Protection / Arbitration / Timing / Governance / Learning)
- C. Measurement Definition (what is measured; units; sampling constraints)
- D. Trigger Condition (logical predicate in measurable terms)
- E. Evidence Artifact Type (waveform / log / config snapshot / timing chart / event payload / environmental record)
- F. Lab Instrument Equivalent (scope/DAQ/DMM naming; channel naming rules)

- G. PMBus/SMBus Mapping (if applicable: device, command, telemetry field, address/bus)
- H. Redfish Projection (if applicable: target schema object/property intent)
- I. DCMI/IPMI Projection (if applicable: power-limit/power-reading/event-style projection intent)
- J. Customer-facing Symptom Label (field observable behavior used in support/RMA)
- K. AI Dataset Label (taxonomy entry: class + attributes; allowed values; confidence rules; “unknown” handling)

This table is mandatory because DV is the **dataset labeling foundation**. DV evidence is invalid if it cannot be mapped to canonical XR terms and dataset labels.

**TABLE 9-1**

Column	Requirement
Canonical Term (XR-VPP)	The only allowed official wording in XR-VPP documents
Alias / Legacy Terms	Supplier/customer common phrases, historical terms, and typical mis-typed variants
Anchor Reference	PMBus/SMBus concept, Redfish metric concept, or ATS/transfer concept reference
Measurement Binding	Which sensor/channel/log proves the term (instrument + node)
Unit & Encoding	Units, scaling, and encoding (raw, calibrated, filtered)
Event Binding	Event code(s) and trigger conditions that represent this term
Pass/Fail Criterion	How the term participates in acceptance (threshold, window, persistence)
AI Label Binding	The dataset label name (taxonomy) used by XR Governance causality drift learning
Notes / Examples	One short example so engineers do not reinterpret the term

### 9.3.3 Versioning rule

The mapping table shall be versioned with semantic changes tracked explicitly:

- Additions: allowed only with explicit rationale and backward compatibility plan
- Renames: prohibited; use deprecation + alias mapping
- Splits/Merges: require traceable migration notes and test-case updates

## 9.4 DV Stages (EVT / DVT / PVT)

**DV is a Roadmap of Capability, Not a One-Time Test.**

### 9.4.1 EVT intent (feasibility + controllability proof)

EVT shall prove:

- The XR-VPP scenario-based power policy is implementable (71W-class servicing higher effective demand via time-sharing and managed transients)
- Basic source arbitration integrity (no unsafe back-feed behavior under defined conditions)
- Minimum evidence pipeline exists (waveforms + logs + event payload schema + mapping table) for future learning

#### 9.4.2 DVT intent (design validation + sampling + drift characterization)

DVT shall prove:

- Scenario coverage across the **Pareto failure-mode families** (reference the Failure Mode / Scenario table and the Pareto chart as DV coverage anchors)
- Characterization of **sensitive timing edges** and drift sources (ESR variance, inrush shaping behavior, OCP/OVP response variability, load collision sensitivity)
- Repeatability and comparability: same test, same definitions, same instruments, same pass/fail criteria across supplier lab and neutral third-party lab

#### 9.4.3 PVT intent (production validation + variance control + pre-qualification readiness)

PVT shall prove:

- Manufacturing variance tolerance: policy stability across unit-to-unit variation
- QA screening hooks: ability to detect abnormal timing signatures early
- Compliance pre-scan readiness: test environment definitions and evidence packaging are consistent with later formal submission expectations (without turning DV into a compliance chapter)

#### 9.4.4 DV Roadmap linkage rule

For each stage, supplier shall deliver a **DV Roadmap Delta** summary:

- What new controllable knobs become available (timing topology options; source arbitration policy options; protection policy ladder options)
- What new evidence fidelity is added (sampling rate, logs, event schema fields)
- What new learning labels become valid (and which remain “experimental / not trusted”)

## 9.5 Evidence Architecture

### What Must Be Captured, How, and How It Feeds AI

#### 9.5.1 Evidence artifacts (mandatory set)

Each DV cycle shall generate the following evidence artifacts, with consistent naming and manifest indexing:

- Waveform package (raw + annotated): key rails, inrush sense, OCP/OVP events, source-switch signals, output port behavior
- Configuration snapshots: firmware build ID, policy configuration, thresholds, timing topology selection, calibration constants
- Governance/event logs: canonical event payloads (XR-native) plus projections (customer-ingestible view)
- Timing charts: standardized timing-diagram artifacts representing sensitive edge windows and controllable intervals
- Environmental record: temperature, input source condition, load profile ID, test bench configuration
- Requirements Traceability Matrix: Spec Requirement ID → Test Case ID → Evidence Artifact ID → Pass/Fail

#### 9.5.2 Timing chart as a standardized DV artifact

A timing chart is a formal evidence summary that must express:

- Defined time offsets between transitions (with named intervals)
- Rising/falling edges with consistent logic-level depiction
- **Sensitive edges identified at signal level** (not only “a time region is critical”)
- For each sensitive edge: allowed drift window, observed drift statistics in DV, and linked failure-mode family/scenario
- Linkage to controllable knobs: which firmware timing parameter(s) or topology selection can tune this edge

Timing charts may be defined for power-on/off and for any scenario window (collision events, transient peaks, ride-through entry/exit, source arbitration decision points). This chapter defines the chart-as-evidence rules; drawing style follows document branding rules.

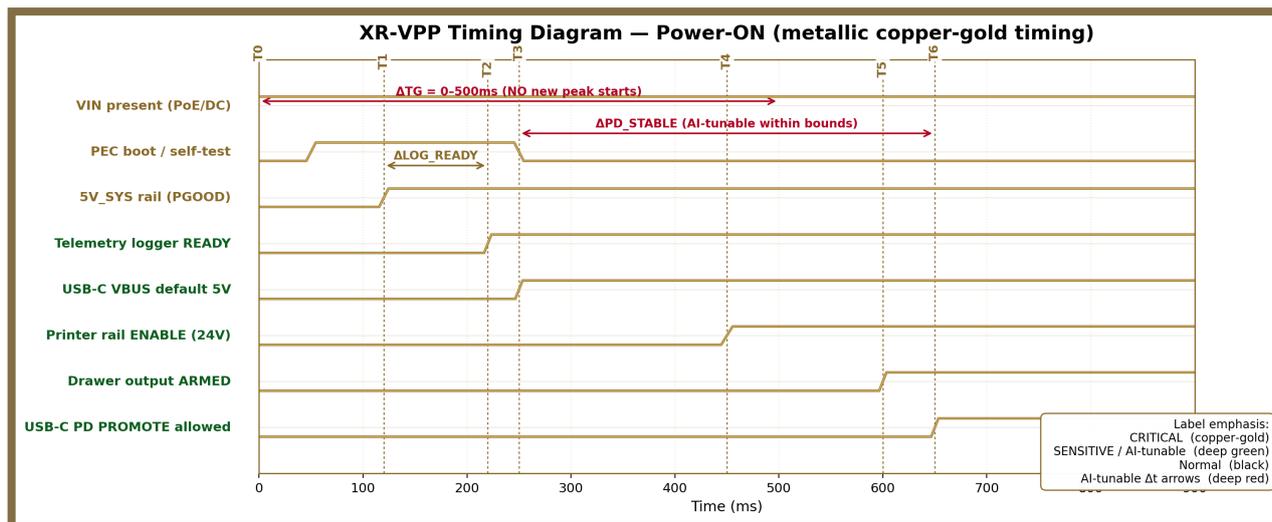


FIGURE 9-2

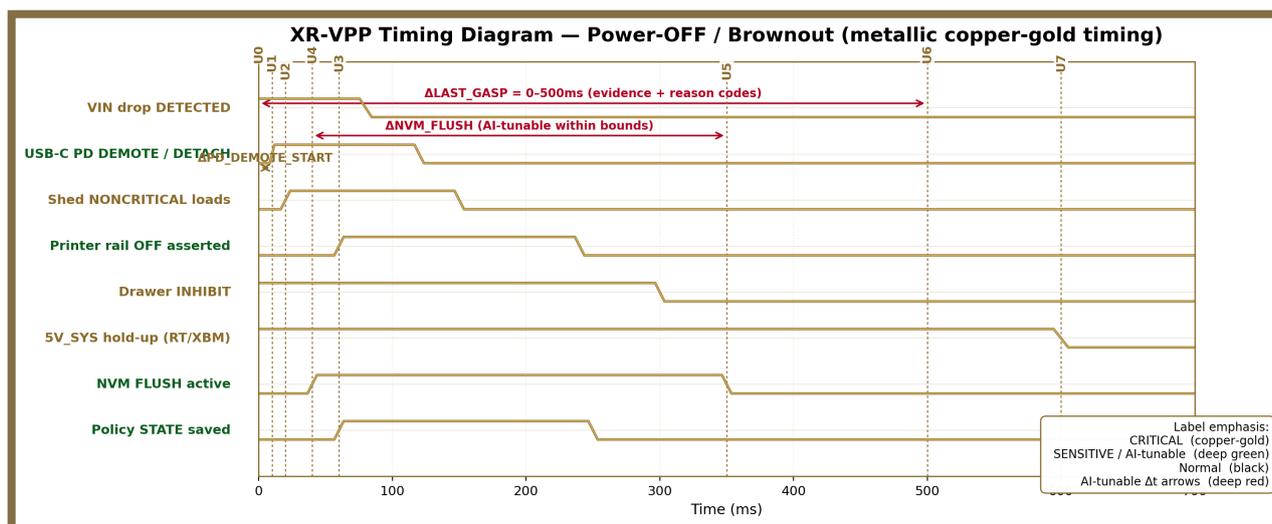


FIGURE 9-3

### 9.5.3 Event payload schema

DV requirement; transport/generation implementation is defined in Firmware Chapter.

DV requires a stable event payload schema because evidence must be machine-ingestible and label-ready. This chapter defines required fields and labeling intent; Firmware Chapter defines transport and generation.

Minimum required event payload attributes:

- Timestamp (monotonic + wall-clock mapping)
- Scenario ID and Active State ID (ties to scenario/state machine definition)
- Source(s) state: qualified/unqualified, selected, inhibited, transition mode
- Output(s) state: port enable, throttle state, negotiated power summary (e.g., USB-C PD contract state)
- Measurements: V/I/P key channels with units and sampling window definition
- Protection events: OCP/OVP/UVP/OTP occurrences with threshold context
- Action: policy ladder action taken, and timing/topology knob used
- Result: recovered/failed, residual risk level, and confidence
- Label: canonical term + dataset label code + label confidence rule

**Note (PDO definition):**

PDO stands for **Power Data Object** in USB Power Delivery. It is an advertised/negotiated capability element used in PD contracts. DV shall treat PD negotiation outcomes as an observable **contract state** that must be logged and mapped consistently when USB-C output is enabled.

**TABLE 9-2**

Field Group	Required Fields (minimum)
Identity	Device SN, Board Rev, FW build ID, DV stage (EVT/DVT/PVT), Lab ID
Time	Global timestamp, local tick, timebase source, sync quality indicator
Context	Input source state, output state, POS scenario ID, collision scenario ID
Trigger	Trigger type (threshold/window/state), trigger condition snapshot
Observables	Key telemetry snapshot (V/I/P/T), status bits, protection flags
Action	Policy action taken, actuator owner (PEC/PD), action result
Evidence Links	Waveform file IDs, timing chart ID, instrument channel map ID
Labels	Failure mode family ID, symptom ID, causality taxonomy tags (minimum dictionary)

**9.5.4 AI learning loop (DV-driven; anti-fragile + anti-error)**

The DV evidence architecture is also the AI training substrate. Therefore, DV shall enforce a **two-layer anti-error mechanism**:

Layer-1: Engineer-entered labels using the canonical mapping table (controlled vocabulary).

Layer-2: Content-based validation using deterministic rules + consistency checks (schema validation, unit checks, allowed-range checks, cross-artifact correlation checks). Any mismatch is raised as a **semantic mismatch defect** and blocks evidence acceptance.

Minimum DV-driven learning flow (per stage):

- Collect DV Evidence Package (waveforms/logs/config/timing charts) with manifest integrity.
- Normalize evidence into canonical schema (mapping table version locked).
- Generate labeled dataset snapshots (train/val/test split rules are declared and reproducible).
- Train/Update model(s) for: scenario classification, drift signature detection, causality-drift scoring, policy recommendation ranking (learning never overrides safety).
- Verify on hold-out DV runs; produce model card: dataset version, label version, metrics, failure cases, and safe-deployment constraints.
- Gate: only models meeting declared acceptance metrics and explainability fields may be promoted to “DV-trusted”.

This section defines the required **process behavior**; tool choices and deliverables are defined in Chapter 10 and Appendix templates.

## 9.6 Acceptance Outputs

### What Supplier Must Deliver Each DV Cycle

Each DV cycle (EVT/DVT/PVT) shall deliver a complete DV Evidence Package that includes:

- DV Summary Report (stage intent, coverage achieved, deviations, design feedback conclusions)
- Updated Semantic Mapping Table (versioned)
- DV Coverage Map (failure-mode families × scenarios × tests × evidence)
- Waveform Package (raw + annotated; with manifest)
- Timing Chart Set (includes sensitive edges and drift windows)
- Governance/Event Log Package (XR-native + customer projection)
- Configuration Snapshot Package (build IDs, policy config, calibration)
- Requirements Traceability Matrix (Spec Requirement ID → Test Case ID → Evidence → Pass/Fail)
- Unresolved Issues List with Severity Classification (including semantic mismatch issues as first-class blockers)

### 9.6.1 Pass/Fail comparability rule (third-party readiness)

A DV claim is not acceptable unless:

- It is expressed in canonical XR terms
- It has defined measurement conditions and pass/fail criteria
- It can be reproduced on a neutral lab bench without supplier-specific naming or undocumented bench shortcuts

- Evidence artifacts are complete and consistent with manifest and traceability matrix.

## 10 DV WORKING MECHANISM & DELIVERABLES

Execution, Third-Party Readiness, Toolchain, and Responsibility

### 10.1 Scope

This chapter defines the execution mechanism that turns the Chapter 9 DV framework into an auditable, repeatable, third-party runnable process. It specifies:

- How DV is executed (supplier lab, neutral third-party lab, customer lab)
- What packages must be produced (evidence package, manifest, traceability, mapping table updates)
- Who owns what (responsibility matrix; review and change control)
- What tools, fixtures, and synchronization rules are required
- How DV outputs become design feedback and roadmap decisions without semantic drift

This chapter is mandatory for all DV stages (EVT / DVT / PVT). Any deviation requires an approved waiver with recorded rationale and impact analysis.

### 10.2 Operating Model (Three-Lab Comparable Execution)

#### 10.2.1 Three execution contexts

DV shall support the same test intent across three contexts, with comparable evidence outputs:

A) Supplier Engineering Lab (primary development DV)

- Purpose: fast iteration, root cause isolation, timing/policy tuning
- Output: full evidence package with raw artifacts and manifest (no summary-only DV)

B) Neutral Third-Party Lab (independence and comparability)

- Purpose: confirm reproducibility; eliminate sampling/operator bias; establish trust baseline
- Output: same evidence package structure and naming rules; lab-specific metadata added

C) Customer Lab / Customer Witness DV (acceptance readiness)

Purpose: acceptance alignment; ensure evidence semantics match customer expectations

Output: reduced scope allowed only if traceability and semantic mapping remain intact

## 10.2.2 Non-negotiable comparability rules

To be considered comparable, any DV run shall satisfy:

- Same Canonical Terms and Mapping Table version (Chapter 9)
- Same Scenario Catalog identifiers (SCN-xx), Failure Mode Families (FM-xx), Timing Profiles (TP-xx), Event Codebook (EVT-xxx)
- Measured quantities, units, sample rate expectations, and pass/fail criteria unchanged (or formally waived)
- Raw evidence preserved (no re-export only)
- Integrity proof (manifest + hashes) included

## 10.3 DV Execution Packages

### 10.3.1 DV Execution Pack (DEP)

Before executing any DV run, the supplier shall produce a DV Execution Pack sufficient for a neutral lab to execute without interpretation. DEP shall include:

- DV Test Matrix (stage-specific: EVT/DVT/PVT) with Test IDs
- Scenario Catalog (SCN-xx): stimulus definitions, device states, collision sequences
- Timing Profile Catalog (TP-xx): parameter sets, allowed ranges, default recommendations
- Measurement Plan: channels, probe points, bandwidth/sample-rate requirements, trigger strategy
- Pass/Fail Criteria: numeric limits and required evidence types per test
- Evidence Plan: which artifacts must be produced per test
- Fixture/Setup Definition: wiring, adapters, load fixtures, cable types/length constraints, grounding guidance
- Event Payload Schema + Event Codebook (EVT-xxx) + log extraction method
- Mapping Table version to be used for this run

DEP is a pre-condition for any third-party DV.

### 10.3.2 Golden Configuration Pack (GCP)

A golden configuration must be defined and frozen per stage to prevent silent drift:

- Firmware build IDs (PEC/EPC, USB-C PD, XR Governance components if enabled)
- Policy ladder configuration version (throttle/shed/RT/transfer rules)
- Calibration constants and sensor offsets
- Hardware revision identifiers (PCB rev, BOM variant, assembly options)
- Power-path option configuration (enabled inputs/outputs, optional modules)

## 10.4 Test Execution Flow (Runbook Standard)

### 10.4.1 Standard run flow (applies to EVT/DVT/PVT)

Step 1 — Pre-Run Control

- Confirm DEP and GCP versions and record them in run header metadata
- Verify instrument calibration status; record instrument IDs/firmware versions
- Verify time sync method (Section 10.5)
- Verify environmental conditions and record baseline (ambient temp, airflow, mounting, fixture)

Step 2 — Baseline Health Check

- Execute Nominal Baseline Test (FM-00) to confirm stable operation
- Verify event payload logging is functional (no missing required fields)

Verify waveform triggers align with log timestamps per chosen sync method

Step 3 — Scenario Execution (SCN-xx)

- Execute tests in DV Test Matrix order
- For each test: capture raw waveforms + logs + config snapshot + timing chart summary artifact

Step 4 — Immediate Post-Run Validation

- Validate required artifacts exist for each Test ID
- Validate manifest completeness and hashes
- Validate FM/SCN/TP/EVT IDs appear consistently across artifacts

Step 5 — Review & Classification

## XR-VPP AI-embedded Power Adapter RFQ

- Run deterministic classification rules (where defined)
- Produce DV Summary Report draft with deviations and suspected mechanisms (without renaming canonical terms)

### Step 6 — Design Feedback Output

Generate Design Feedback Record (DFR) per issue: symptom, evidence references, suspected mechanism, recommended actions, expected DV confirmation test

## 10.4.2 Drift and false-trigger management (required)

DV shall explicitly characterize:

- Threshold drift (UVP/OCP/OVP/OTP) across temperature and manufacturing variance
  - Timing drift across conditions (rise/fall time changes due to ESR, inrush shaping, collision sensitivity)
  - False trigger rate and recovery behavior (policy ladder correctness)
- All drift claims must tie to evidence artifacts and be labeled consistently.

## 10.5 Instrumentation and Time Synchronization Requirements

### 10.5.1 Time alignment requirement

DV evidence must support alignment between waveform captures and event logs. Each DV run shall choose one method and declare it in metadata:

#### A) External Trigger Alignment (preferred)

- Dedicated trigger output to scope/DAQ
- Event log includes corresponding trigger marker event (EVT-TRIG) with time\_us

#### B) Shared Time Reference Alignment

- If XR-VPP provides RTC/wall time, record wall\_time\_utc in logs and capture instrument system time
- Declare tolerance ( $\pm X$  ms) and validate in baseline test

#### C) Monotonic Correlation Alignment

- Use monotonic time\_us plus defined correlation procedure (known toggling signature captured in both domains)
- Method must be documented and demonstrated

### **10.5.2 Minimum measurement tool expectations (supplier-facing)**

Supplier shall provision or arrange access to tools sufficient to capture DV evidence repeatably:

- Oscilloscope with adequate bandwidth; differential probes as required
- Current measurement (probe or shunt+amplifier) for inrush/step load
- Electronic load(s) for scripted profiles and fast transients
- PoE test capability (injector/analyzer or equivalent)
- USB-C PD analyzer (PDO/contract visibility)
- Thermal measurement (thermocouples and/or thermal camera)
- DAQ/log capture workstation capable of storing raw artifacts without lossy conversion

Any limitation must be declared as DV limitation with impact assessment and third-party confirmation plan.

## **10.6 Evidence Package Structure, Naming, Manifest, and Integrity**

### **10.6.1 DV Evidence Package (DEP-OUT)**

Each DV run shall output a single DV Evidence Package directory/archive that is complete and self-contained:

#### A) Reports

- DV\_Summary\_Report (PDF)
- Deviations\_and\_Waivers (PDF)
- Design\_Feedback\_Records (PDF or structured document)

#### B) Matrices and Tables

- Requirements\_Traceability\_Matrix (XLSX/CSV)
- DV\_Test\_Matrix (XLSX/CSV)
- Semantic\_Mapping\_Table (XLSX/CSV)

## XR-VPP AI-embedded Power Adapter RFQ

- Scenario\_Catalog (XLSX/CSV)
- Timing\_Profile\_Catalog (XLSX/CSV)
- Event\_Codebook (PDF + machine-readable mapping if provided)

### C) Raw Evidence

- Waveforms (raw instrument files + exported plots)
- Event Logs (JSONL/CBOR as specified)
- Configuration snapshots (text/JSON)
- Timing charts (PDF/PNG) as standardized artifacts
- Environmental records (CSV/JSON)

### D) Manifest and Integrity

- Manifest listing all artifacts, sizes, hashes (SHA-256), timestamps, tool versions, and run metadata
- Run header includes DEP version, GCP version, firmware build IDs, hardware rev, options enabled

## 10.6.2 Naming convention (mandatory)

All artifacts shall include:

{Project}{Stage}{RunID}{DeviceID}{BuildID}{TestID}{ArtifactType}\_{Timestamp}

## 10.6.3 Manifest requirements

The manifest shall include:

- Package identity (Project, Stage, RunID, Lab identity, Date/time)
- Device identity (DeviceID, HW revision, options enabled)
- Software identity (build\_id(s), policy config version, schema\_version)
- Artifact inventory (filename, type, size, SHA-256, tool+version, TestID linkage)
- Integrity statement: raw artifacts included and unchanged since capture

Missing artifacts are failures unless formally waived.

## 10.7 Responsibility Matrix (Role Map)

### 10.7.1 Required roles (minimum)

Supplier must assign owners per run and record in DV package:

- A) Power Hardware Owner (Supplier)
- B) Firmware Owner — PEC/EPC (Supplier)
- C) Firmware Owner — USB-C PD (Supplier)
- D) Governance/Learning Integration Owner (Supplier or XR team as contracted)
- E) Validation Engineer (Supplier)
- F) Third-Party Lab Coordinator (Neutral)
- G) XR-VPP Spec Owner / Customer Representative (Your side)

### 10.7.2 Decision rights

The following require DV re-run or documented equivalence justification:

- Firmware build changes affecting timing/policy/protection/arbitration/PD behavior
- Hardware revision changes affecting power-path/sensing/threshold/thermal behavior
- Timing Profile Catalog changes (TP parameters/allowed ranges)
- Event payload schema changes or meaning changes
- Mapping table canonical term changes (renames prohibited; alias/deprecation only)
- Any change impacting pass/fail criteria

## 10.8 Toolchain Requirements

### Data Handling, Parsing, Reproducibility, and AI Training Enablement

#### 10.8.1 Data handling and reproducibility

Supplier shall provide repeatable method to:

- Extract logs from XR-VPP
- Export waveforms while retaining raw instrument formats
- Generate plots without altering raw evidence

- Generate manifest hashes automatically
- Produce single archive suitable for third-party transfer

### **10.8.2 Minimum software expectations (must output; not must use)**

DV process must output:

- CSV/XLSX tables (RTM, mapping table, scenario catalog, timing catalog)
- JSONL/CBOR logs per schema
- SHA-256 hashes for all artifacts
- Deterministic run metadata record

Supplier tool choice (Python/Node/proprietary) is not mandated, but steps must be documented so a neutral lab can reproduce evidence package generation without non-shareable internal scripts.

### **10.8.3 Recommended open toolchain (informative; China/Vietnam-friendly)**

To reduce risk and enable consistent training across sites, the following open tools are recommended (or equivalents):

- Dataset/versioning: DVC (or Git-LFS)
- Experiment tracking: MLflow (or equivalent)
- Labeling UI (if manual review needed): Label Studio (or equivalent)
- Training runtime: PyTorch (or equivalent), export to ONNX for deployment portability
- Validation scripts: schema validation + unit checks + cross-artifact correlation checks (mandatory capability, regardless of tool)

Toolchain is acceptable if it produces the required outputs, preserves raw evidence, and supports repeatable training/verification runs.

## **10.9 Design Feedback Workflow**

From Evidence to Actions to Roadmap

### **10.9.1 Design Feedback Record (DFR) format (mandatory)**

Each issue shall generate a DFR including:

- Canonical term(s) and mapped IDs (FM/SCN/TP/EVT)
- Evidence references (artifact IDs, timestamps, waveform markers)
- Symptom and measurable impact
- Suspected mechanism hypotheses (design-side) without renaming canonical terms
- Proposed corrective actions (HW, FW timing, policy ladder changes)
- Proposed verification test(s) with required closure evidence
- Roadmap implication: Base vs Flagship/Redundancy-ready relevance

### **10.9.2 Roadmap gate closure rule**

A roadmap increment is ready only when:

- DV evidence completeness achieved for defined scope
- Semantic alignment stable (no uncontrolled term drift)
- Timing profile tunability bounded and justified by evidence
- Dataset labeling consistent and repayable for learning iterations
- AI verification outputs meet declared acceptance metrics and constraints

## **10.10 Third-Party DV Engagement Model (Practical Execution)**

### **10.10.1 Neutral lab execution checklist**

Before sending to a neutral lab, supplier shall provide:

- DEP + GCP
- Fixture drawings and wiring diagrams
- Instrumentation channel list and trigger strategy
- Expected evidence outputs and naming/manifest rules
- Contact list for rapid clarification (without changing DV semantics)

### **10.10.2 Handling discrepancies between labs**

If supplier lab and neutral lab disagree:

- Treat first as semantic/evidence mismatch (mapping/instrument/trigger alignment), not immediately as design failure
- Produce reconciliation report with side-by-side evidence references and one canonical interpretation
- Any changes go through change control and may require re-DV depending on impact

## 10.11 Compliance Pre-Test Integration

DV as Qualification Preparation

DV is designed as pre-qualification preparation. Compliance activities may run in parallel, but DV shall:

- Capture environmental and configuration parameters relevant to later submission
- Preserve evidence semantics consistent with third-party reporting
- Prevent “pass by bench trick” by enforcing reproducibility and manifest integrity

# 11 APPENDIX A — SUPPLIER ACCEPTANCE MATRIX AND VALIDATION REQUIREMENTS

## 11.1 Purpose

This appendix defines supplier-facing acceptance criteria to validate XR-VPP functionality, including ride-through (RT), peak loading support (Preset A), output regulation, governed behavior (Qi disable / USB-C throttle), and evidence logging.

Figures and thresholds below define **test intent and pass/fail structure**. Final numeric limits shall be locked in the “Electrical Release” revision.

## 11.2 Definitions (Normative)

- **Rated Power (Steady-State):** continuous output capability under thermal steady state and defined ambient conditions.
- **Peak Power/Event:** time-limited transient load condition bounded by a peak envelope.
- **RT Window (Ride-Through):** time interval during which outputs shall remain within required envelopes during input dropout/brownout conditions.
- **RT-500 @ 65W:** ride-through capability sustaining required outputs for 500 ms while delivering up to 65W steady load condition during the event, subject to policy ladder actions.

## 11.3 Test Conditions (Supplier Standard Setup)

### A.3.1 Environmental

- Ambient temperature: TBD (e.g., 25°C nominal; additional corners TBD)
- Airflow: fanless / natural convection unless otherwise specified
- Mounting condition: TBD (free-air or mounted to metal plate/stand)

### A.3.2 Instrumentation

- Oscilloscope (bandwidth TBD) for rail droop, recovery, and peak waveform capture
- Power analyzer for input/output power and efficiency
- Thermal measurement (thermocouples or IR) for hotspot tracking

- Event log extraction tool (TBD interface path: RJ45/USB-C/service port)

### A.3.3 Load Equipment

- Programmable electronic load supporting static + dynamic profiles
- Dynamic transient load profile capability for peak tests

## 11.4 Acceptance Matrix (Supplier Pass/Fail Table)

**Note:** Values marked TBD shall be finalized at Electrical Release. The table is structured so suppliers can quote and execute validation planning immediately.

### 11.4.1 Output Regulation and Basic Operation

**TABLE 11-1**

Test ID	Scenario	Setup	Stimulus	Pass Criteria	Evidence / Log Code
A-REG-19V-01	19V output regulation	Nominal input source	Step load (TBD)	19V within $\pm 5\%$ , no oscillation	LOG: REG_OK / REG_WARN
A-START-01	Power-up sequencing	Any valid source	Power on	Deterministic startup, no protection pre-trigger	LOG: PWR_ON_SEQ
A-SWITCH-01	Source arbitration	Multiple sources present (as allowed)	Remove active source, present alternate	Controlled switch-over per PEC rules	LOG: SRC_ARB, SRC_SWITCH

### 11.4.2 RT (Ride-Through) Verification — RT-500 Flagship

**TABLE 11-2**

Test ID	Scenario	Setup	Stimulus	Pass Criteria	Evidence / Log Code
A-RT-500-01	RT dropout event (primary)	Load = 65W (TBD distribution)	Input dropout duration = 500 ms	19V remains within defined RT envelope (TBD droop/recovery); no uncontrolled reset	LOG: RT_ENTER, RT_EXIT, RT_PASS
A-RT-500-02	RT + policy actions	USB-C enabled; Qi enabled	Trigger RT window	Qi disabled first; USB-C throttle applied if needed; 19V preserved	LOG: QI_OFF, USBC_THROTTLE, RT_POLICY
A-RT-500-03	RT recovery behavior	Same as above	Restore input	Exit RT mode deterministically; outputs recover within recovery limits	LOG: RT_RECOVER

**RT Envelope Definition (TBD):**

- Allowable droop: TBD (e.g., max droop %, max duration)
- Recovery time: TBD
- No oscillatory behavior during event/recovery

### 11.4.3 Peak Loading Support — Preset A

**TABLE 11-3**

Test ID	Scenario	Setup	Stimulus	Pass Criteria	Evidence / Log Code
A-PEAK- A-01	Peak transient event	Steady load near rated	Apply dynamic peak (e.g., printer transient)	Output remains within peak envelope (TBD droop, duration); recovery within limits	LOG: PEAK_ENTER, PEAK_EXIT, PEAK_PASS
A-PEAK- A-02	Peak + output priority	USB-C enabled; Qi enabled	Apply peak profile	Ladder executed: Qi off → USB-C throttle → preserve 19V; no immediate shutdown unless safety triggered	LOG: QI_OFF, USBC_THROTTLE, PEAK_POLICY
A-PEAK- A-03	Peak persistence handling	Same as above	Extend peak beyond window	Controlled behavior: maintain within limits or enter safe-state deterministically	LOG: PEAK_TIMEOUT, SAFE_STATE

**Preset A Envelope Definition (TBD):**

- Peak magnitude limit: TBD (W/A)
- Peak duration window: TBD (ms)
- Allowable droop and recovery: TBD
- Priority actions allowed: Qi off, USB-C throttle, controlled safe-state

### 11.4.4 Option Behavior — USB-C and Qi

**TABLE 1 1-4**

Test ID	Scenario	Setup	Stimulus	Pass Criteria	Evidence / Log Code
A-USBC-THR-01	USB-C throttle mode	USB-C enabled	Trigger constrained budget	USB-C enters low-power mode; 19V preserved	LOG: USBC_THROTTLE
A-QI-OPT-01	Qi option enable/disable	Qi enabled	Trigger constraint	Qi disabled as first-shed load	LOG: QI_OFF
A-OPT-REC-01	Option recovery	Options previously shed	Restore normal budget	Options recover only under policy permission; no oscillation	LOG: OPT_RECOVER

### 11.4.5 Logging, Evidence, and Traceability

**TABLE 1 1-5**

Test ID	Scenario	Setup	Stimulus	Pass Criteria	Evidence / Log Code
A-LOG-01	Minimal power SMART log	XR Governance disabled	Induce RT + peak + switch events	PEC log persists required events; exportable via interface	LOG: PEC_SMART_OK
A-LOG-02	Governance evidence narrative	XR Governance enabled	Same sequence	Evidence includes cause, action, rail status, timestamps	LOG: GOV_EVID_OK

## 11.5 Mandatory Log/Event Code Set (Minimum)

The following event markers shall exist (PEC baseline + Governance enhanced):

- PWR\_ON\_SEQ, PWR\_OFF\_SEQ
- SRC\_ARB, SRC\_SWITCH
- RT\_ENTER, RT\_EXIT, RT\_POLICY, RT\_RECOVER
- PEAK\_ENTER, PEAK\_EXIT, PEAK\_POLICY, PEAK\_TIMEOUT
- QI\_OFF, USBC\_THROTTLE, OPT\_RECOVER
- FAULT\_OCP, FAULT\_OVP, FAULT\_UVLO, FAULT\_OTP, FAULT\_SURGE

- SAFE\_STATE

Each log entry shall include: timestamp, active source, rail status summary, and policy action summary.

## 11.6 Supplier Deliverables

Supplier shall provide:

- Test report with scope covering A.4 matrix items
- Waveform captures for RT and peak tests
- Thermal report summary under rated and peak envelopes
- Evidence log exports (PEC baseline and Governance enabled where applicable)

## 12 APPENDIX B — RT PROFILES AND PEAK PROFILES (MEASURABLE WAVEFORM SPECIFICATIONS)

### 12.1 Ride-Through (RT) Test Profiles — Input Dropout / Brownout

#### 12.1.1 Test Setup (Common)

- **Active outputs:** 19V rail enabled (mandatory). USB-C and Qi shall be tested per option scenarios.
- **Load condition:**
  - **RT-500 Flagship condition:** Total steady load = **65W** (distribution per A.7.2).
  - Optional extended test at rated steady load TBD (future release).
- **Instrumentation:**
  - Measure 19V rail at output connector (sense at load if possible).
  - Record input voltage/current and internal bus if available.
  - Capture time correlation with log codes.

#### 12.1.2 Load Distribution (for repeatability)

Unless otherwise specified by SKU:

- **19V rail:** 55W steady
- **USB-C (if enabled):** 10W steady (or low-power mode threshold if throttled)
- **Qi (if enabled):** 0–10W as configured (Qi is expected to shed first under RT)

Supplier may propose alternate distribution only if total equals 65W and the distribution is disclosed and approved.

#### 12.1.3 RT Profile RT-DROP Series (Hard Dropout)

These profiles simulate complete loss of input power for a defined duration.

### 12.1.3.1 RT-DROP-500 (Flagship)

- **Initial condition:** stable operation  $\geq 60$  s at 65W steady load
- **Stimulus:** input voltage goes from nominal to **0V** within  $\leq 2$  ms
- **Dropout duration:** **500 ms  $\pm$  5 ms**
- **Recovery:** input returns to nominal within  $\leq 10$  ms, then remains stable  $\geq 60$  s

#### Pass criteria (19V rail):

- No uncontrolled shutdown/reset of 19V rail (no “flatline”).
- Allowable 19V droop envelope during event:
  - Minimum voltage: **TBD** (recommended placeholder: not below 17.5V)
  - Droop duration beyond  $\pm 5\%$  band: **TBD** (recommended placeholder:  $\leq 120$  ms cumulative)
- Recovery: return into  $\pm 5\%$  band within **TBD** (recommended placeholder:  $\leq 150$  ms)

#### Policy behavior expectations:

- **Re** If Qi is enabled  $\rightarrow$  **must disable** during RT window if required to preserve 19V.
- USB-C may throttle to low-power mode per policy ladder; throttle event must be logged.

quired logs:

RT\_ENTER, RT\_EXIT, plus QI\_OFF and/or USBC\_THROTTLE if actions taken.

### 12.1.3.2 RT-DROP-250 (Engineering / Backward Compatibility)

Same as RT-DROP-500 but dropout duration = **250 ms  $\pm$  5 ms**.

Used to validate behavior under shorter ride-through expectations or lower-capacity SKUs.

### 12.1.3.3 RT-DROP-100 (Legacy / Minimum)

Same as above but dropout duration = **100 ms  $\pm$  5 ms**.

## 12.1.4 A.7.4 RT Profile RT-BROWN Series (Brownout / Sag)

These profiles simulate degraded input rather than total loss.

### 12.1.5 RT-BROWN-1 (Two-Step Sag)

- **Initial:** stable operation  $\geq 60$  s
- **Stimulus:** input drops from nominal to **V\_sag** within  $\leq 5$  ms
- **Hold:** remain at V\_sag for **500 ms  $\pm$  5 ms**
- **Recover:** return to nominal within  $\leq 10$  ms

**V\_sag definition (by input type):**

- For DC input (External DC/XBM): **V\_sag = 0.6  $\times$  V\_nom**
- For PoE-derived DC after PD stage: apply sag at the **pre-conversion DC input point** if test access exists; otherwise emulate via programmable PoE source to reduce available power to equivalent sag.

**Pass criteria:**

- 19V rail remains within RT envelope or executes graceful policy actions; no oscillation.
- Logs include RT markers + policy actions.

## 12.2 A.7.5 Input Source Applicability Notes (No Loopholes)

The RT profiles shall be executed under each applicable input mode for the SKU:

- **PoE mode:** using programmable PoE PSE/emulator where possible.
- **External DC mode:** using programmable DC source.
- **XBM mode:** using XBM test fixture or approved emulator that matches XBM output behavior.

Supplier may use emulation fixtures, but must document equivalency.

## 12.3 Peak Profiles — Preset A (Measurable Dynamic Load

### Waveforms)

#### 12.3.1 Purpose

Preset A targets real POS transient behavior (e.g., printer activation / dark print segments / cutter events) where short peaks occur on 19V or downstream rails.

#### 12.3.2 Peak Test Setup (Common)

- **Input mode:** run at least one peak profile under PoE worst-case budget and one under External DC.
- **Baseline steady load:**  $P_{base} = 55W$  on 19V (unless otherwise specified).
- **Peak event load is applied on 19V rail** unless the SKU defines a dedicated 24V rail in future variants.

### 12.3.3 Peak Waveform Definitions (Preset A Series)

#### 12.3.3.1 PEAK-A1 (Single Pulse Peak)

- **Baseline:** 55W steady for  $\geq 30$  s
- **Rise time:** baseline  $\rightarrow$  peak within  $\leq 2$  ms
- **Peak level:**  $P_{peak} = 72W$  (rated steady reference) OR  $I_{peak}$  TBD (recommended placeholder: +3A equivalent on target rail)
- **Peak duration (dwell):**  $200$  ms  $\pm$   $10$  ms
- **Fall time:** peak  $\rightarrow$  baseline within  $\leq 5$  ms
- **Repeat:** 1 event per 10 s, total 20 events

#### Pass criteria:

- 19V droop during pulse remains within peak droop envelope: TBD (recommended placeholder: not below 18.0V)
- Recovery into  $\pm 5\%$  band within TBD (recommended placeholder:  $\leq 80$  ms)
- No protection latch unless safety boundary truly violated
- Evidence logs: PEAK\_ENTER, PEAK\_EXIT, optionally USBC\_THROTTLE / QI\_OFF

#### 12.3.3.2 PEAK-A2 (Burst Peaks)

Simulates repeated printer bursts.

- **Baseline:** 55W steady for  $\geq 30$  s
- **Pulse definition:** same as PEAK-A1 but dwell =  $120$  ms  $\pm$   $10$  ms
- **Burst:** 5 pulses with **500 ms spacing** between pulses
- **Burst interval:** 10 s between bursts
- **Total bursts:** 10

#### Pass criteria:

- No cumulative droop runaway; no oscillation
- Optional loads may shed/throttle per ladder; actions must be logged.

### 12.3.3.3 PEAK-A3 (Step-Load Plateau)

Simulates sustained higher draw during continuous printing.

- **Baseline:** 55W steady for  $\geq 30$  s
- **Step up:** baseline  $\rightarrow$  **P\_step = 72W** within  $\leq 5$  ms
- **Hold:** **2.0 s  $\pm$  0.1 s**
- **Step down:** return to baseline within  $\leq 10$  ms
- **Repeat:** 10 cycles with 10 s rest

#### Pass criteria:

- If platform cannot hold 72W steady without violating Type-4 budget, it shall apply policy actions in order: Qi off  $\rightarrow$  USB-C throttle  $\rightarrow$  preserve 19V
- Must not enter uncontrolled shutdown; if safe-state is necessary, must be controlled and logged: SAFE\_STATE

### 12.3.4 Policy Hooks Under Peak (Mandatory Behavior)

During PEAK-A profiles, policy ladder shall apply:

- Preserve 19V continuity
- Qi off first (if enabled)
- USB-C throttle as needed
- Controlled safe-state only if safety boundaries require it

## 12.4 Recommended Placeholder Values vs Final Lock

To avoid blocking supplier quoting and early validation, this appendix defines **measurable profiles now**, with **pass/fail envelopes labeled TBD** for final lock.

**Rule:** Supplier must still run the exact waveform profiles (drop times, dwell, repeats).

Final voltage droop limits and recovery limits will be locked at “Electrical Release”.

# 13 APPENDIX C XR-VPP — TARGET COST BOM BREAKDOWN

(Hard Cap: USD \$15 EXW target)

**Assumption:** 5k–20k annual volume class, supplier may reuse existing platform.

**Goal:** Supplier must propose architecture/BOM choices to meet **Total COGS ≤ \$15**.

## 13.1 Core BOM Targets (supplier must fit within these buckets)

**TABLE 13-1**

Bucket	What supplier must include	Target (USD)
<b>1. Power front-end (selected input)</b>	Any one of: PoE-PD front end <b>or</b> DC-in front end <b>or</b> XBM-assist front end (supplier chooses baseline) incl. basic protection/inrush	
<b>2. Main conversion stage</b>	48–57V (if used) to system bus + regulated outputs (supplier decides topology), incl. magnetics/FETs/controller	
<b>3. Output connectors (mechanical)</b>	Connectors only (RJ45 / DC jack / XBM / 19V out / USB-C) — supplier decides which are base vs optional, but must quote adders	
<b>4. PEC (Power Embedded Controller) + sensing</b>	MCU + voltage/current/temp sensing + watchdog + basic event log NVM	
<b>5. RT window + peak support circuitry</b>	Ride-through detect + hold-up strategy + throttle hook support (implementation can be firmware-only if feasible)	
<b>6. PCB + SMT + test</b>	PCB fab + assembly + functional test (power-up, protection trip, basic burn-in policy)	
<b>7. Mechanical set (top+base)</b>	Housing + mounting features + finishing (supplier chooses process: stamped Al, extrusion, plastic+spreader, die-cast if they can)	
<b>8. Final assembly + yield reserve</b>	Screws/pads/adhesives/gasket (if used) + rework/yield allowance	
<b>TARGET COST</b>		<b>\$8.00</b>

Supplier instruction (put this line into RFQ):

“Supplier shall propose BOM and manufacturing plan that meets the above bucket targets and guarantees total EXW cost ≤ USD 8.00. Supplier may choose architecture and materials to achieve the cap, but must preserve the functional intents and safety constraints listed below.”

### 13.2 Option Adders (quote separately; total must still meet \$15)

These are **not allowed to be silently included**. Supplier must quote as adders.

**TABLE 13-2**

Option	Definition	Target Adder (USD)
PoE Type-4 (bt) PD upgrade	From base (af/at or DC-in) to bt PD front end	
USB-C ≥65W enabled	USB-C PD controller + power path rated ≥65W	
Qi module ready	Coil + driver + mechanical seat + cable	
XBM assist interface	Keyed connector + detect/ID/EN + harness retention	
ADC12 die-cast upgrade	Replace low-cost housing with ADC12 die-cast + CNC + anodize	
Extended telemetry/export	Additional memory/PHY/isolation for data export	
<b>TARGET COST</b>		<b>USD7.00</b>

### 13.3 Non-Negotiable Functional Intents (supplier cannot “cost-cut away”)

#### 13.3.1 Safety & protection (must exist regardless of architecture)

- OCP / OVP / UVLO / OTP / inrush handling must exist as **deterministic protection behavior**.
- Protection must be implemented in hardware/firmware such that unsafe override is impossible.

#### 13.3.2 PEC independence

- Device must **still work** if XR Governance/AI features are disabled.  
(PEC is the real-time authority for sequencing and protection.)

### 13.3.3 RT / Peak intent (implementation free, intent fixed)

- Provide **RT window behavior** with **throttle policy hook** and **peak transient handling mode**.
- Supplier may implement RT via supercap / output holdup / staged throttle / “graceful brownout” approach — but must show measured waveform in DV.

### 13.3.4 Architecture freedom, but must be explicit

Supplier must deliver:

- A block diagram of their proposed cost-down architecture
- BOM with unit costs
- Which features are **base** vs **optional adders**
- A DV test list proving protection + RT/peak behaviors

### 13.3.5 Supplier Deliverables Required in Quote (so they can't handwave)

Ask them to return:

- **Costed BOM** (line-item, with alternates)
- **Manufacturing assumptions** (PCB layers, assembly/test steps, yield)
- **Mechanical process choice** (must justify how they hit \$3.00 set cost)
- **Waveform proof plan**: RT window + peak transient tests (even if simulated first)
- **Compliance strategy** (what they can claim at this cost; what is extra)

### 13.3.6 One-liner you can paste into RFQ email

We are enforcing a hard EXW target of USD 15 for the base XR-VPP module. Attached is the bucketed should-cost target. You may choose architecture/materials to achieve it, but you must preserve PEC safety authority, deterministic protection, and RT/peak intent. Quote base + option adders explicitly with a costed BOM.

## 14 APPENDIX D DELIVERABLE TEMPLATES & INSTRUCTIONS (MASTER INDEX)

### 14.1 Purpose

This appendix defines the mandatory deliverable templates and the exact instructions for how to fill, package, name, and submit them. These templates are the operational implementation of Chapter 9 (Validation Framework) and Chapter 10 (DV Working Mechanism). Unless explicitly waived, every DV cycle (EVT/DVT/PVT) shall deliver the complete 14 template set in a single DV Evidence Package.

### 14.2 DV Evidence Package Naming & Folder Convention (MANDATORY)

#### 14.2.1 Package name (archive or folder)

`XR-VPP_DV_{STAGE}{RunID}{LabID}{DeviceFamily}{HWRev}{FWBuild}{YYYYMMDD-HHMM}`

- STAGE: EVT / DVT / PVT
- RunID: DV-0001, DV-0002...
- LabID: SUP (supplier) / 3P (third-party) / CUS (customer)
- DeviceFamily: XR-VPP-200 / XR-VPP-300 / XR-VPP-ALL
- HWRev: HW-A1, HW-B0...
- FWBuild: PEC-1.2.3\_PD-0.9.1\_XRG-0.3.0
- Timestamp: 20260112-1930

#### 14.2.2 Folder structure (fixed)

01\_REPORTS/  
02\_MATRICES\_TABLES/  
03\_SCENARIO\_TIMING/  
04\_LOGS\_DATASET/  
05\_WAVEFORMS/

06\_CONFIG\_SNAPSHOTS/

07\_MANIFEST\_INTEGRITY/

### 14.2.3 Manifest & integrity

- Manifest file: **07\_MANIFEST\_INTEGRITY/manifest\_sha256.csv**
- Required: filename, size, sha256, artifact\_type, TestID, FM/SCN/TP/EVT IDs, generator\_tool, tool\_version, timestamp

## 14.3 DV Evidence Package: Naming & Folder Rules (MANDATORY)

**TABLE 14-1**

Item	Requirement (exact)
Package name	<b>XR-VPP_DV_{STAGE}{RunID}{LabID}{DeviceFamily}{HWRev}{FWBuild}{YYYYMMDD-HHMM}</b>
STAGE	EVT / DVT / PVT
RunID	DV-0001, DV-0002...
LabID	SUP (supplier) / 3P (neutral third-party) / CUS (customer / witness)
DeviceFamily	XR-VPP-200 / XR-VPP-300 / XR-VPP-ALL
HWRev	HW-A1, HW-B0...
FWBuild	PEC-x.x.x_PD-x.x.x_XRG-x.x.x (include all applicable FW domains)
Folder structure	<b>01_REPORTS/ 02_MATRICES_TABLES/ 03_SCENARIO_TIMING/ 04_LOGS_DATASET/ 05_WAVEFORMS/ 06_CONFIG_SNAPSHOTS/ 07_MANIFEST_INTEGRITY/</b>
Manifest file	<b>07_MANIFEST_INTEGRITY/manifest_sha256.csv</b>
Manifest minimum columns	filename, artifact_type, TestID, FM/SCN/TP/EVT IDs, size, sha256, generator_tool, tool_version, timestamp
Integrity rule	Evidence is invalid if required artifacts exist only as summaries without raw files and hash manifest.

## 14.4 Master Deliverable Index (WHAT / WHERE / WHO / WHEN)

**TABLE 14-2**

ID	Deliverable (template name)	Output file name (fixed)	Folder	Primary owner	EVT/ DVT/ PVT
14-4	DV Summary Report	DV_Summary_Rep ort.docx (or .pdf)	01_REPORTS	Validation Lead	Y
14-5	Deviations & Waivers Log	DV_Deviations_Wa ivers.docx (or .pdf)	01_REPORTS	Validation Lead	Y
14-6	Design Feedback Records (DFR)	DFR.xlsx	01_REPORTS	Power + FW Leads	Y
14-7	DV Coverage Map (FM×SCN×TestID)	DV_Coverage_Map .xlsx	02_MATRICES_T ABLES	Validation Lead	Y
14-8	Requirements Traceability Matrix (RTM)	RTM.xlsx	02_MATRICES_T ABLES	Spec Owner + Validation	Y
14-9	Semantic Mapping Table (canonical + aliases)	Semantic_Mapping _Table.xlsx	02_MATRICES_T ABLES	Spec Owner + Domain Leads	Y
14-10	Seed Mapping Table v0.1 (baseline)	Semantic_Mapping _Seed_v0.1.xlsx	02_MATRICES_T ABLES	Spec Owner	Y
14-11	Scenario Catalog (SCN-xx)	Scenario_Catalog. xlsx	03_SCENARIO_T IMING	Validation + FW	Y
14-12	Timing Profile Catalog (TP-xx)	Timing_Profile_Cat alog.xlsx	03_SCENARIO_T IMING	FW Lead	Y
14-13	Timing Chart Set (artifact)	Timing_Charts.pdf (or .pptx)	03_SCENARIO_T IMING	FW + Validation	Y
14-14	Event Log File Format Spec	EventLog_FileForm at_SPEC.pdf	04_LOGS_DATA SET	FW + Data Owner	Y
14-15	Dataset Schema (machine-ingestible)	dataset_schema.js on	04_LOGS_DATA SET	Data Owner	Y
14-16	Policy Action Enumerations (MVD)	policy_action_enu m_v0.1.csv	04_LOGS_DATA SET	XR Gov Lead	Y
14-17	Source State Enumerations (MVD)	source_state_enu m_v0.1.csv	04_LOGS_DATA SET	Power Lead	Y
14-18	Output State Enumerations (MVD)	output_state_enu m_v0.1.csv	04_LOGS_DATA SET	Power + PD Lead	Y



14-15	dataset_schema.js on	Machine-ingestible schema with enums linking to 14-12~14-16; required/nullable rules
14-16	policy_action_enum	Each action: code + exact sentence + safety_class + required evidence + constraints
14-17	source_state_enum	Each state: code + entry/exit predicates + prohibited combos (backfeed risk)
14-18	output_state_enum	Each state: code + port behavior + PD contract/PDO summary rules (if USB-C enabled)
14-19	protection_event_enum	Each event: code + threshold context + latch/retry behavior + required waveform markers
14-20	causality_taxonomy_mvd	Minimum dictionary enabling causality drift labeling across stages
14-21	Raw waveforms	Native instrument files + exported plots; must reference TestID and edge markers
14-22	Config snapshots	Build IDs + policy config + calibration constants + option flags; immutable per run
14-23	Manifest	SHA-256 for every artifact; completeness check; missing items are failures unless waived

## 14.6 DV Package Naming

### 14.6.1 DV Summary Report (Template)

**TABLE 14-4**

Section	Minimum required content	Mandatory
Cover / Run	Project/Stage/RunID/LabID/DeviceID(s)/HW	Yes
Header	Rev/BuildID(s)/PolicyConfigVer/EventSchemaVer/MappingVer/Date+TZ/Prepared–Reviewed–Approved	
AI Readiness Statement	Dataset volume + label completeness vs stage gate; declare PASS/FAIL + gaps	Yes
Coverage Summary	TestID ↔ ReqID ↔ SCN/TP ↔ Evidence IDs ↔ Result (Pass/Fail)	Yes
Causality / Drift Highlights	Top causal chains + drift sources + cross-condition deltas (with evidence pointers)	Yes
Deviations / Waivers	List Waiver IDs + scope + impact on comparability / AI usability	Yes
References	Manifest + RTM + Mapping + Codebooks/Schemas/Validators (file IDs)	Yes

### 14.6.2 Deviations & Waivers Log (Template)

**TABLE 14-5**

WaiverID	Scope (Req/Test/Artifact)	Deviation / Waiver description (short)	Impact	Approval (By/Date)

### 14.6.3 Design Feedback Records (DFR) (Template)

**TABLE 14-6**

DFR_ID	FM/SCN/TP	Symptom (measurable)	Evidence IDs	Suspected mechanism (controlled phrase)	Proposed action	Verify TestID(s)

### 14.6.4 DV Coverage Map (Template)

**TABLE 14-7**

FM_Family	ScenarioID (SCN-xx)	TimingProfileID (TP-xx)	TestID	Required evidence (WF/LOG/TCHART/CFG)	Result	Notes

### 14.6.5 Requirements Traceability Matrix (RTM) (Template)

**TABLE 14-8**

RequirementID	Requirement (short)	TestID(s)	Evidence Artifact ID(s)	Pass/Fail	Notes


### 14.6.6 Semantic Mapping Table (Template)

**TABLE 14-9**

Canonical XR Term	Category	Measurement definition	Trigger condition	Evidence type	Instrument/channel alias	PMBus/SMBus map	Mgmt projection (Redfish/DCMI/IPMI)	Customer symptom label	AI label code

### 14.6.7 Seed Mapping Table v0.1 (Starter Rows)

**TABLE 14-10**

Alias / Source term	Canonical XR Term	Category	Where seen (supplier/lab/customer)	Notes
inrush current	INRUSH_I	Protection/Timing	scope label	
brown-out	INPUT_DROOP	Input/Timing	customer symptom	
power good	PWRGD	Output/Timing	firmware log	

### 14.6.8 Scenario Catalog (SCN-xx) (Template)

**TABLE 14-11**

ScenarioID	Name	Stimulus/sequence (short)	Preconditions	Expected behavior	Causal windows {t_start_us,t_end_us,+signals}	Drift windows {t_start_us,t_end_us,+features}	Required evidence WF+LOG+TCHART+CFG	Linked FM

### 14.6.9 Timing Profile Catalog (TP-xx) (Template)

**TABLE 14-12**

TimingProfileID	Parameter name	Default	Allowed range	Units	Linked edge/window	Related SCN-xx	Notes

### 14.6.10 Timing Chart Set (Artifact Index Template)

**TABLE 14-13**

TCHART_ID	ScenarioID	TimingProfileID	Edge IDs	Signals/channels	Windows (named)	Limits (drift/pass-fail)	FileRef (PDF/PNG)

### 14.6.11 Event Log File Format Spec (Template)

**TABLE 14-14**

Item	Specification	Mandatory
Primary format	JSONL (one record per line, UTF-8)	Yes
Optional binary	CBOR (same fields)	Optional
Time base	time_us monotonic; optional wall_time_utc ISO8601	Yes
File naming	{...}{ArtifactType=LOG}_{Timestamp}	Yes
Line discipline	No multi-line; stable key order recommended	Yes
Compression (optional)	zstd/gzip allowed if declared in manifest	Optional

### 14.6.12 Dataset Schema (Machine-ingestible) (Template)

**TABLE 14-15**

Field	Type	Meaning (short)	Required
schema_version	string	dataset schema version	Yes

project_id	string	XR-VPP	Yes
stage	enum	EVT/DVT/PVT	Yes
run_id	string	RUN-xxx	Yes
lab_id	string	SupplierLab/ThirdPartyLab/CustomerLab	Yes
device_id	string	DEV-xxxxx	Yes
hw_rev	string	PCB/mech revision	Yes
bom_variant_id	string	BOM/AVL variant	Yes
eco_id	string	ECO/ECN ref or NA	Yes
test_id	string	TST-xxx	Yes
scenario_id	string	SCN-xx	Yes
timing_profile_id	string	TP-xx	Yes
time_us	uint64	monotonic timestamp	Yes
event_code	string	EVT-xxx	Yes
severity	enum	INFO/WARN/ERROR/FATAL	Yes
event_domain	enum	INPUT/OUTPUT/PROTECTION/TIMING/PD/THERMAL/GOV	Yes
policy_action	enum	see Table 14-4m	Yes
outcome	enum	RECOVERED/DEGRADED/FAILED/UNKNOWN	Yes
evidence_refs	object	artifact IDs + segments	Yes

### 14.6.13 Policy Action Enumerations (MDV)

**TABLE 14-16**

policy_action	Meaning	Notes
NONE	No action	
THROTTLE	Reduce negotiated/allowed power	
SHED_LOAD	Disable non-critical output/port	
SWITCH_SOURCE	Change input source	Requires qualification rules
ENTER_RT	Enter ride-through mode	
EXIT_RT	Exit ride-through mode	
RETRY	Retry/renegotiate	PD/Source retry
DERATE_THERMAL	Thermal derating	
LATCH_OFF	Latch off output	Safety condition
CLEAR_FAULT	Clear fault state after conditions	

### 14.6.14 Source State Enumerations (MDV)

**TABLE 14-17**

source_state	Meaning
DISABLED	Not enabled by config
PRESENT	Physically present / detected
QUALIFYING	In qualification timer/window
QUALIFIED	Meets stability criteria
SELECTED	Actively selected as input
INHIBITED	Blocked by policy/holdoff
TRANSITIONING	In transfer / arbitration
FAULTED	Fault latched for source

### 14.6.15 Output State Enumerations (MDV)

**TABLE 14-18**

output_state	Meaning
OFF	Port disabled
ON	Port enabled and stable
NEGOTIATING	PD contract negotiation
LIMITED	Power limited by policy
THROTTLED	Throttling active
SHED	Load shed applied
RECOVERING	Recovery sequence
FAULTED	Output fault latched

### 14.6.16 Protection Event Enumerations (MDV)

**TABLE 14-19**

protection_event	Meaning
OCP_WARN	Over-current warning
OCP_TRIP	Over-current trip
OVP_TRIP	Over-voltage trip
UVP_TRIP	Under-voltage trip
OTP_WARN	Over-temperature warning
OTP_TRIP	Over-temperature trip

INRUSH_LIMIT	Inrush limiting active
BACKFEED_DETECT	Backfeed path detected

### 14.6.17 Causality Taxonomy (Minimum) (MDV)

**TABLE 14-20**

Node	Required fields	Example values
cause_node	{cause_class,cause_subclass}	ESR_VARIATION / CABLE_DROP / SOURCE_INSTABILITY
mechanism_node	{mech_class,control_state}	INRUSH_SHAPING_DELAY / QUAL_TIMER / ORING_BODY_DIODE
symptom_node	{morphology,magnitude,duration}	DROOP / OVERSHOOT / OSCILLATION / RETRY_STORM
action_node	{policy_action,knob_name,knob_value}	THROTTLE(TP_DELTA=+200us) / SWITCH_SOURCE(QUAL=80ms)
outcome_node	{result,residual_risk}	RECOVERED/DEGRADED/FAILED + risk score

### 14.6.18 Raw Waveform Package (Scope / Native)

**TABLE 14-21**

Item	Minimum requirement	Mandatory
Native raw files	Original scope/DAQ formats preserved	Yes
Exported plots	PNG/PDF aligned to raw captures	Yes
Channel set	Key rails + inrush sense + source-select + port behavior	Yes
Sampling/BW note	Record sample rate/bandwidth/probe type in ENV/metadata	Yes
Markers	Edge IDs + window markers referenced by TCHART/CAUSE/DRIFT	Yes

### 14.6.19 Configuration Snapshots (Build / Policy / Calibration)

**TABLE 14-22**

Snapshot	Format	Minimum content	Mandatory
Firmware build IDs	text/JSON	all component build IDs + git hash if available	Yes
Policy config	JSON	policy ladder + thresholds + timing profile selection	Yes
Calibration constants	JSON	sensor offsets + shunt factors + temp calibration	Yes
HW identity	text	PCB rev + BOM variant + option modules	Yes

### 14.6.20 Manifest + Hashes (Template)

**TABLE 14-23**

Field	Meaning	Required
package_identity	project/stage/run_id/lab_id/date_tz	Yes
device_identity	device_id/hw_rev/bom_variant_id/eco_id	Yes
software_identity	build_ids + policy_config_version + schema_versions	Yes
artifact_inventory	list(path,type,size,sha256,tool,tool_version,linked_test_id)	Yes
integrity_statement	raw evidence included + unchanged since capture	Yes